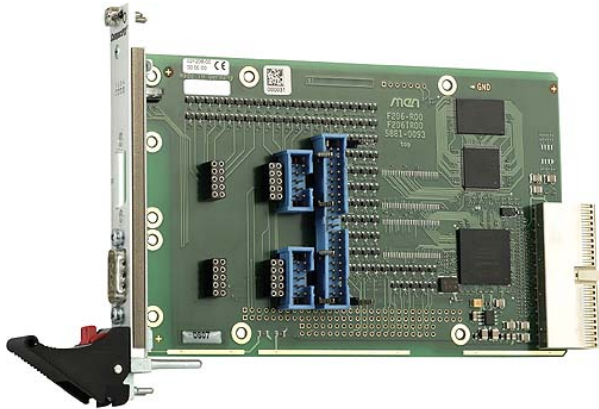


# F206 - 3U CompactPCI® Octal UART for SA-Adapters™



- **Octal 16450 UART**
- **RS232/422/485, isolated/not isolated**
- **Physical layer via SA-Adapters™**
- **Large receive and transmit FIFOs**
- **Very high data rates up to 2 Mbits/s**
- **Full handshake support**
- **Hardware flow control for RS485 half duplex**
- **Also for other protocols like HDLC**
- **-40 to +85°C with qualified components**

The F206 is a universal octal UART based on 3U CompactPCI®. The physical layer can be realized individually for each channel by means of SA-Adapters™. SA-Adapters™ are small universal boards providing the physics for legacy serial I/O, fieldbus interfaces and other small I/O functions. Most SA-Adapters™ use 9-pin D-Sub connectors which are accessible at the front panel. Alternatively, the adapter can be connected to the front panel via ribbon cable. The SA concept allows to add additional I/O interfaces to the F206, enhancing flexibility with regard to the line transceivers and isolation requirements. Two SA-Adapters™ can be mounted directly on the F206 (single-slot solution), the other maximum six adapters need more front-panel space and are connected to the carrier via ribbon cable. Especially useful adapters for the F206 are isolated and non-isolated adapters for RS232, RS422 and RS485 interfaces. Different types can be used on one F206.

The octal UART is realized by means of an FPGA. The register set is fully 16450 compatible, even with larger, 60-byte FIFOs. The FPGA is loaded automatically after power-up from a 2MB standard NOR Flash device. It is also possible to access this Flash from the CompactPCI® bus to update its contents. There is a primary and a secondary FPGA filling in the Flash. Normally just the secondary code is used. Only in case of a fault during the update process the primary contents allow another update of the Flash from the CompactPCI® bus. Optionally also a 16MB SDRAM can be installed to complement the functions of the FPGA. This DRAM can be used for example as a large buffer memory for more complex protocols. The F206 is designed for use in rugged environments. For example, all components are specified for an operation temperature of -40 to +85°C.

## Technical Data

### UARTs

- Up to eight UARTs
- Accessible via on-board connectors
- Physical interface at front panel using SA-Adapters™ via 10-pin ribbon cable
- Different variations with SA-Adapters™ possible:
  - RS232
  - RS422
  - RS485
- Data rates up to 2 Mbits/s
- 60-byte transmit/receive buffer
- Handshake lines: full support; lines depend on SA-Adapters™

### FPGA

- Standard factory FPGA configuration:
  - Main bus interface
  - 16Z054\_SYSTEM - System unit
  - 16Z025\_UART - UART controller (controls COM10..COM13)
  - 16Z025\_UART - UART controller (controls COM14..COM17)
  - 16Z045\_FLASH - Flash interface
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

### Miscellaneous

- Four status LEDs

### Local PCI Bus

- 32-bit/33-MHz, 3.3V V(I/O)
- Compliant with PCI Specification 2.2

### CompactPCI® Bus

- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- Peripheral slot
- V(I/O): +3.3V

### Electrical Specifications

- Supply voltage/power consumption:
  - +5V (-3%/+5%), current depends only on mounted SA-Adapters™
  - +3.3V (-3%/+5%), > 500mA typ.
- MTBF: 308,000h @ 40°C (derived from MIL-HDBK-217F)

### Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Single 3U front panel slot for up to two UARTs
- Up to two supplementary front panel slots required for overall eight UARTs
- Front panel: aluminum with 1 handle
- Weight: 95g

### Environmental Specifications

- Temperature range (operation):
  - -40..+85°C (qualified components)
  - Airflow: min. 10m<sup>3</sup>/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

### Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

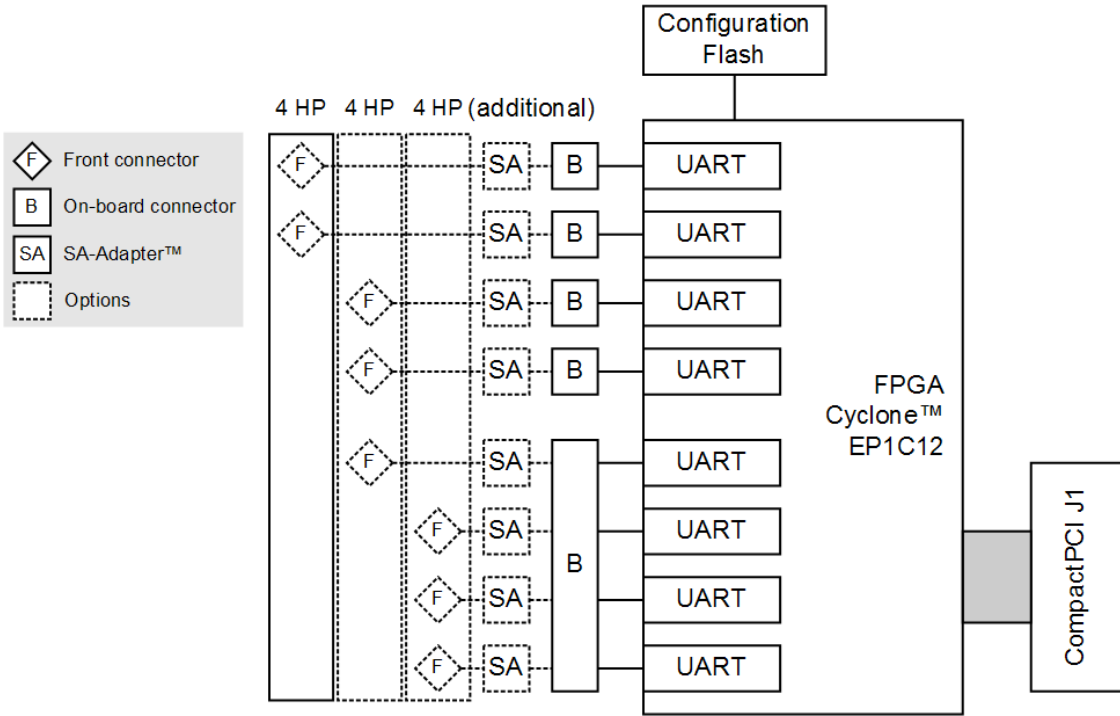
### EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

### Software Support

- Driver software for Windows®, Linux, VxWorks®, QNX®
- Flash update tools for Windows®, Linux, VxWorks®
- For more information on supported operating system versions and drivers see Software.

### Diagram



## Configuration & Options

### Standard Configurations

Article No.	No. of UARTs	Front Panel	FPGA content	Operation Temperature
02F206-00	2 (via SA-Adapters™)	4 HP, 2 D-Sub	8 UARTs	-40..+85°C
02F206-00 + 05F206-02	5 (via SA-Adapters™)	8 HP, 5 D-Sub	8 UARTs	-40..+85°C
02F206-00 + 05F206-03	8 (via SA-Adapters™)	12 HP, 8 D-Sub	8 UARTs	-40..+85°C

### Options

#### Physical Layers

- Via up to eight SA-Adapters™
- Different variations possible through FPGA IP cores and SA-Adapters™:
  - RS232
  - RS422
  - RS485
  - IBIS master/slave
  - CAN bus
  - HDLC
  - Binary I/O
  - InterBus-S
  - Other physical layers dependent on FPGA configuration
  - [Option matrix showing possible IP cores and SA-Adapters™ \(PDF\)](#)

#### Mechanical

- 4, 8 or 12 HP front panel dependent on number of SA-Adapters™
  - 4 HP with 2 on-board SA-Adapters™
  - 8 HP with 5 SA-Adapters™
  - 12 HP with 8 SA-Adapters™
- One-piece front panel
- Different front panel cut-outs possible

**Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.**

## FPGA

### FPGA Capabilities

- FPGA Altera® Cyclone™ EP1C12
  - 12,060 logic elements
  - 239,616 total RAM bits
- For UART functions
- Simple functional updates via software
- 2MB Flash for FPGA configurations

### Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- Depending on the hardware platform, SA-Adapters™ can be used to realize the physical lines.

### MEN IP Cores

- MEN has a large number of standard IP cores to choose from.
- Examples:
  - IDE (e.g. PIO mode 0, UDMA mode 5)
  - UARTs
  - CAN bus
  - Display control
  - Fast Ethernet (10/100Base-T)
  - ...
- For IP cores developed by MEN please refer to our IP core overview.
  - [IP Core compare chart \(PDF\)](#)
- MEN also offers development of new (customized) IP cores.

### Third-Party IP Cores

- Third-party IP cores can also be used in combination with MEN IP cores.
- Examples:
  - [www.altera.com](http://www.altera.com)
  - [www.opencores.org](http://www.opencores.org)

### FPGA Design Environment

- Altera® offers free download of Quartus® II Web Edition
  - Complete environment for FPGA and CPLD design
  - Includes schematic- and text-based design entry
  - Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
  - SOPC Builder system generation software
  - Place-and-route, verification, and programming
- [Altera® Quartus® II Web Edition FPGA design tool](#)

## Ordering Information

### Standard Hardware

**02F206-00** 4 HP FPGA-based UART interface for direct connection of 2 UARTs (2 SA-Adapters™ to be ordered separately) at front, 8 UARTs standard FPGA content plus space for user-defined functions, -40..+85°C with qualified components

### SA-Adapters

**08SA01-00** RS232, not optically isolated, 0..+60°C  
**08SA02-00** RS422/485, half duplex, optically isolated, 0..+60°C  
**08SA02-01** RS422/485, full duplex, optically isolated, 0..+60°C  
**08SA02-07** RS422/485, full duplex, optically isolated, -40..+85°C screened  
**08SA03-00** RS232, optically isolated, 0..+60°C  
**08SA03-01** RS232, optically isolated, -40..+85°C screened  
**08SA22-00** IBIS master SA-Adapter™, -40..+85°C screened  
**08SA22-01** IBIS slave SA-Adapter™, -40..+85°C screened

### Miscellaneous

**05F206-02** Kit (4 HP front panel and cables) for connection of 3 additional UART SA-Adapters™ to F206, F206N - SA-Adapters™ to be ordered separately (cannot be combined with 05F206-03)  
**05F206-03** Kit (8 HP front panel and cables) for connection of 6 additional UART SA-Adapters™ to F206, F206N - SA-Adapters™ to be ordered separately (cannot be combined with 05F206-02)

### Software: Linux

**13Z025-90** Linux native driver (MEN) for 16Z025\_UART, 16Z057\_UART and 16Z125\_UART  
**13Z055-90** Linux native driver (MEN) for 16Z055\_HDLC with TCP/PPP support  
**13Z100-91** Linux FPGA update tool (MEN)

### Software: Windows

**13F206-70** Windows® driver installation package Installset (MEN) for F206  
**13Z100-70** Windows® FPGA update tool (MEN)

### Software: VxWorks

**13Z025-60** VxWorks® native driver (MEN) for 16Z025\_UART, 16Z057\_UART and 16Z125\_UART  
**13Z100-60** VxWorks® FPGA update tool (MEN)

### Software: QNX

**13Z025-40** QNX® native driver (MEN) for 16Z025\_UART and 16Z125\_UART

### Documentation

**20F206-00** F206 User Manual  
**21APPN009** Application Note: 16Z025\_UART and 16Z125\_UART under Linux  
**22Z025-ER** 16Z025\_UART Errata

**For the most up-to-date ordering information and direct links to other data sheets and downloads, see the F206 online data sheet under » [www.men.de](http://www.men.de).**

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