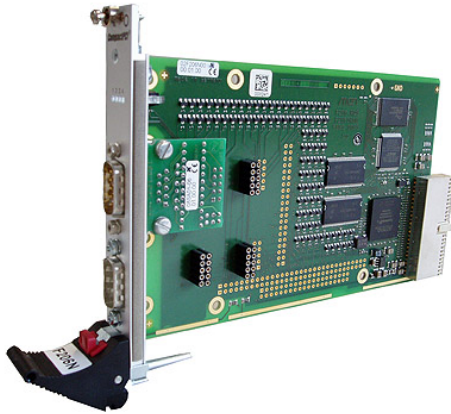


F206N - 3U CompactPCI® Nios® II Slave Board



- **32-bit/33-MHz CompactPCI®**
- **Peripheral slot function**
- **FPGA 12,000 LEs (approx. 144,000 gates)**
- **Nios® II soft processor**
- **32 MB SDRAM, 2 MB Flash**
- **Flexible FPGA-Flash structure**
- **Open platform FPGA development package**
- **Support of Wishbone and Avalon® bus**
- **-40 to +85°C with qualified components**

The F206N is a 3U CompactPCI® card with an on-board Altera® Cyclone™ FPGA and the integrated Nios® II soft processor. It is designed for final use in volume in an application and it acts at the same time as the standard FPGA development platform for this application.

Due to its multitude of directly accessible I/O pins the F206N can be used as a universal FPGA platform. With the Nios® II CPU inside the FPGA, the F206N can for example act as an intelligent slave on the CompactPCI® bus. In any case the F206N supports a nearly endless range of applications. Examples may include functions such as an intelligent 8-channel CAN controller with DMA and local protocol stack, real-time Ethernet controller, analog front end with DSP-like pre-computing, intelligent counter, intelligent HDLC interface etc.

The Cyclone™ FPGA acts as the main controller. It

supports a 32-bit/33-MHz CompactPCI® bus, controls the SDRAM memory and has read/write access to the Flash memory. The special FPGA-Flash structure provides initial programming using a boundary scan interface and later, with a configured FPGA, the device may be updated at any time with data from the CompactPCI® bus. The FPGA also controls four status LEDs and up to 79 user-defined I/O pins.

A total of 32MB soldered SDRAM and 2MB Flash back the potential computing functionality of the F206N.

The F206N is designed for use in rugged environments.

For example, all components are specified for an operation temperature of -40 to +85°C.

For development of the application MEN provides a Nios® - CompactPCI® open platform FPGA development package that includes a sample design with an internal PCI system unit, integrating the standard Wishbone and the Altera® Avalon® bus.

Technical Data

CPU

- Nios® II soft processor
 - 33MHz

Memory

- 512 bytes instruction cache and 512 bytes data cache integrated in Nios® II
- 32MB SDRAM system memory
 - Soldered
 - 133MHz memory bus frequency
- 2MB boot Flash

I/O

- One RS232 UART (COM10)
 - D-Sub connector at front panel
 - Data rates up to 115.2kbits/s
 - 60-byte transmit/receive buffer
 - Handshake lines: full support
 - For debugging
- Three 10-pin connectors
 - For FPGA-controlled functions
 - For use of one additional SA-Adapter™
 - One receptacle for direct SA-Adapter™ connection at the front
 - Two receptacles for direct connection of long SA-Adapters™ at the front (instead of short SA-Adapters™)
 - Different physical layers through SA-Adapters™: RS232, RS422, RS485, Ethernet, CAN bus, binary I/O

FPGA

- Standard factory FPGA configuration:
 - Nios® II soft processor
 - 16Z014_PCI - PCI to Wishbone interface
 - 16Z052_GIRQ - Global Interrupt Controller (Nios®)
 - 16Z052_GIRQ - Global Interrupt Controller (CPU)
 - 16Z069_RST - Reset Controller
 - 16Z043_SDRAM - SDRAM controller (32MB)
 - 16Z045_FLASH - Flash interface
 - 16Z025_UART - UART controller (controls COM10)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

Miscellaneous

- Four user LEDs, FPGA-controlled

Local PCI Bus

- 32-bit/33-MHz, 3.3V V(I/O)
- Compliant with PCI Specification 2.2

CompactPCI® Bus

- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- Peripheral slot
- 32-bit/33-MHz PCI
- V(I/O): +3.3V
- Only one slot required on 3U CompactPCI® backplane
- More supplementary CompactPCI® slots required depending on SA-Adapters™

Electrical Specifications

- Supply voltage/power consumption:
 - +5V (-3%/+5%), current depends only on mounted SA-Adapters™
 - +3.3V (-3%/+5%), 500mA typ.
- MTBF: 308,000h @ 40°C (derived from MIL-HDBK-217F)

Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Single 3U front panel slot for up to two 9-pin D-Sub connectors
- Weight: 165g

Environmental Specifications

- Temperature range (operation):
 - -40..+85°C (qualified components)
 - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

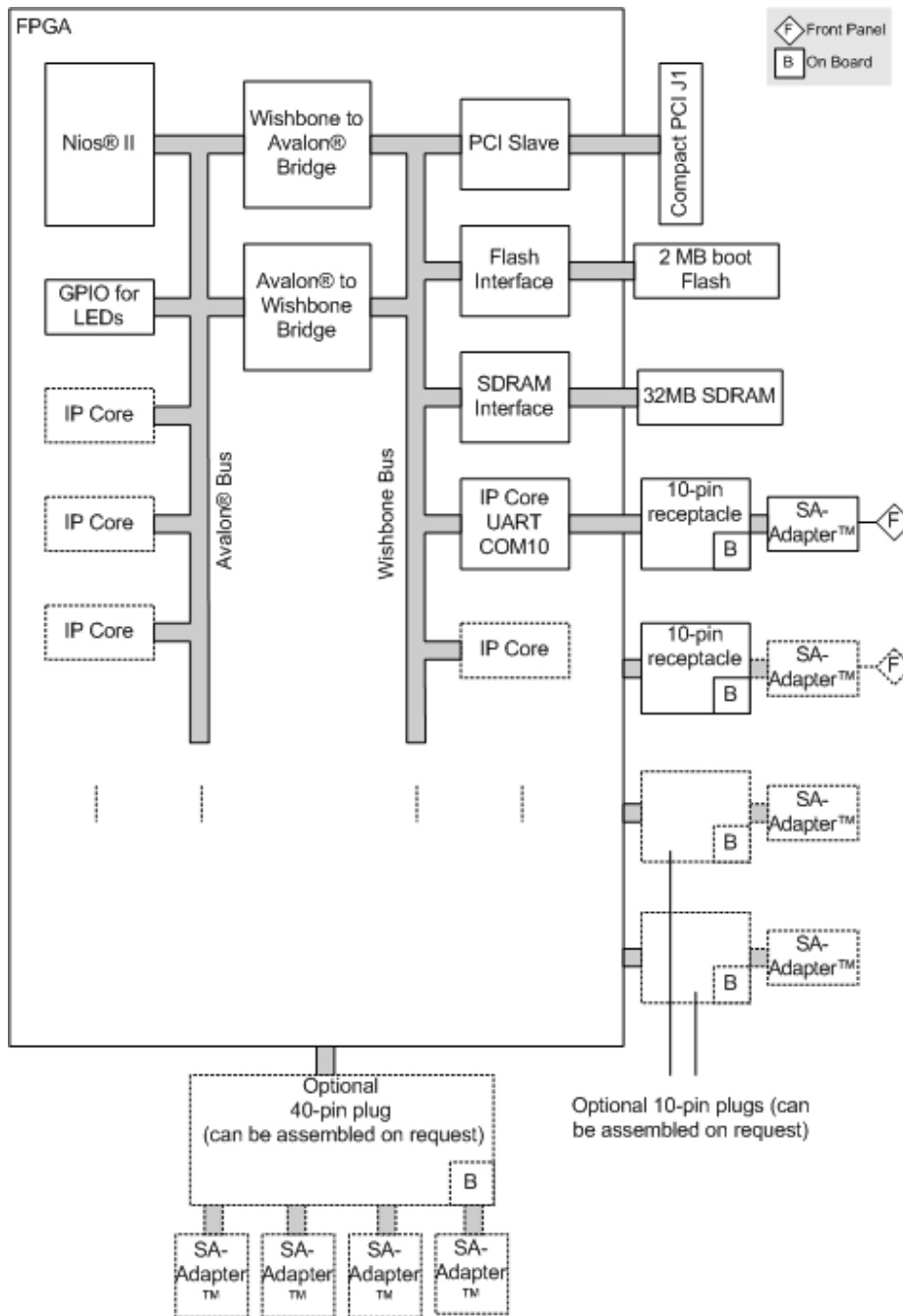
EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support

- Nios® sample design for Quartus® II development tools
- Flash update tools for Windows®, Linux, VxWorks®
- Driver software depending on implemented FPGA functions
- For more information on supported operating system versions and drivers see Software.

Diagram



Configuration & Options

Standard Configurations

Article No.	Preconf.UARTs	Physical Line Adapters	Front Panel	FPGA Content	Operation Temperature
02F206N00	1 RS232	1 (via SA-Adapters™)	4TE, 2 DSUB	1 UART, Nios®	-40..+85°C

Options

I/O

- Two 10-pin plugs for on-board connection of two additional SA-Adapters™ via ribbon cable (on request)
- One 40-pin plug for on-board connection of up to four additional SA-Adapters™ via ribbon cable (on request)
- Different physical layers via SA-Adapter™ controlled by FPGA

FPGA

- Customized IP core functions configurable by customer or MEN

Mechanical

- 4, 8 or 12HP front panel dependent on number of SA-Adapters™ (8 or 12HP on request)
- One-piece front panel
- Different front panel cut-outs for audio, USB etc.

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

FPGA

FPGA Capabilities

- FPGA Altera® Cyclone™ EP1C12 (optional EP1C20)
 - 12,060 logic elements
 - 239,616 total RAM bits
 - Logic elements of Nios® II soft processor (standard version): approx. 3500
- Connection
 - Functions can be linked to Wishbone or Avalon® bus
 - Available pin count: 79 I/O lines
 - Functions available via I/O connectors
- MEN offers an Open Platform FPGA Development Package as well as Flash update tools for different operating systems.

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- Depending on the hardware platform, SA-Adapters™ can be used to realize the physical lines.

MEN IP Cores

- MEN has a large number of standard IP cores to choose from.
- Examples:
 - IDE (e.g. PIO mode 0, UDMA mode 5)
 - UARTs
 - CAN bus
 - Display control
 - Fast Ethernet (10/100Base-T)
 - ...
- For IP cores developed by MEN please refer to our IP core overview.
 - [IP Core compare chart \(PDF\)](#)
- MEN also offers development of new (customized) IP cores.

Third-Party IP Cores

- Third-party IP cores can also be used in combination with MEN IP cores.
- Examples:
 - www.altera.com
 - www.opencores.org

FPGA Design Environment

- Altera® offers free download of Quartus® II Web Edition
 - Complete environment for FPGA and CPLD design
 - Includes schematic- and text-based design entry
 - Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
 - SOPC Builder system generation software
 - Place-and-route, verification, and programming
- [Altera® Quartus® II Web Edition FPGA design tool](#)

Ordering Information

Standard Hardware

- 02F206N00** F206N, 3U CompactPCI®, 1-slot FPGA-based intelligent Nios® II slave board, 32MB DRAM, 2MB Flash, 1x RS232 (08SA01-06) mounted, FPGA for user-defined functions, operation temperature -40..+85°C
- 16F206N00** Nios®-CompactPCI® Open Platform FPGA Development Package (MEN) (without Altera® Quartus® II)

SA-Adapters

- 08SA01-00** RS232, not optically isolated, 0..+60°C
- 08SA02-00** RS422/485, half duplex, optically isolated, 0..+60°C
- 08SA02-01** RS422/485, full duplex, optically isolated, 0..+60°C
- 08SA02-07** RS422/485, full duplex, optically isolated, -40..+85°C screened
- 08SA03-00** RS232, optically isolated, 0..+60°C
- 08SA03-01** RS232, optically isolated, -40..+85°C screened
- 08SA08-00** CAN ISO high-speed, optically isolated, 0..+60°C
- 08SA08-01** CAN ISO high-speed, optically isolated, -40..+85°C screened
- 08SA09-01** SA9, serial interface adapter, InterBus-S master interface, optically isolated, 0..+60°C
- 08SA15-00** 8 digital I/O channels, -40..+85°C with qualified components, no RoHS
- 08SA22-00** IBIS master SA-Adapter™, -40..+85°C screened
- 08SA22-01** IBIS slave SA-Adapter™, -40..+85°C screened

FPGA Packages

- 16F206N00** Nios®-CompactPCI® Open Platform FPGA Development Package (MEN) (without Altera® Quartus® II)

Software: Linux

- 13Z025-90** Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
- 13Z100-91** Linux FPGA update tool (MEN)

Software: Windows

- 13Z100-70** Windows® FPGA update tool (MEN)

Software: VxWorks

- 13Z025-60** VxWorks® native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
- 13Z100-60** VxWorks® FPGA update tool (MEN)

Software: QNX

- 13Z025-40** QNX® native driver (MEN) for 16Z025_UART and 16Z125_UART

Software: FPGA

- 16F206N00** Nios®-CompactPCI® Open Platform FPGA Development Package (MEN) (without Altera® Quartus® II)

Documentation

- 20F206N00** F206N User Manual
- 21APPN009** Application Note: 16Z025_UART and 16Z125_UART under Linux
- 21F206N00** F206N Programmer's Guide
- 22Z025-ER** 16Z025_UART Errata

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the F206N online data sheet under > www.men.de.

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