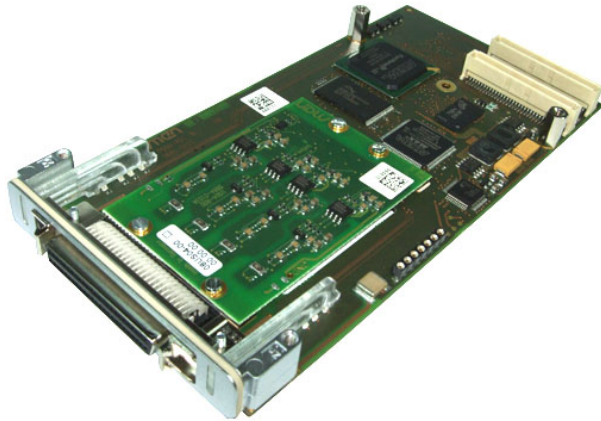


P506 - Quad CAN Bus Interface PMC



- **32-bit/33-MHz PMC**
- **Full CAN/Extended CAN**
- **4 independent channels**
- **ISO high-speed coupling**
- **Up to 1 Mbit/s data transfer rate**
- **CANopen master and slave support**
- **CAN Layer 2 support**
- **Isolation between channels**
- **Compliant to ISO 11898-1 and ISO 11898-2**
- **-40 to +85°C with qualified components**

The P506 is a 32-bit/33MHz PMC with four CAN interfaces. They support CAN Protocol Version 2.0A/B, standard and extended data frames, remote frames, 0..8 bytes data length and a programmable data rate of up to 1 Mbit/s.

The P506 is based on the USM™ concept. USM™ Universal Submodules make PMC modules more flexible than ever. The CAN bus interfaces are realized via four IP cores implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The

corresponding line drivers are realized on the USM™ which is simply plugged on the P506.

The module is suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC in telecommunication, industrial, medical, transportation or aerospace applications. It offers long-term availability for at least 10 years and is qualified for operation in the extended temperature range.

Technical Data

CAN Interface

- Compliant to ISO 11898-1 and ISO 11898-2
- Four channels
- CAN Protocol Version 2.0A/B
 - Standard and extended data frames
 - 0..8 bytes data length
 - Programmable data rate up to 1 Mbit/s
- Support for remote frames
- 5 receive buffers (FIFO-scheme)
- 3 transmit buffers with prioritization
- Maskable identifier filter
- Programmable loop-back mode for self-test operation
- Signaling and interrupt capabilities for receiver and transmitter error states

Memory

- 32MB SDRAM memory
 - Soldered
 - DDR2
 - 132MHz memory bus frequency
 - FPGA-controlled
- 2MB non-volatile Flash
 - For FPGA data and Nios® firmware
 - FPGA-controlled

FPGA

- Standard factory FPGA configuration:
 - Main bus interface
 - Interrupt controller, SMBus controller
 - [16Z029_CAN](#) - CAN Controller
 - [16Z043_SDRAM](#) - SDRAM controller
 - [16Z045_FLASH](#) - Flash interface
 - [16Z034_GPIO](#) - GPIO controller
 - [16Z034_PWM](#) - PWM Pulse Width Modulation
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

PMC Characteristics (PCI)

- Compliant with PCI Specification 2.2
- 32-bit/33-MHz, 3.3V V(I/O)
- Target

Peripheral Connections

- Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector

Electrical Specifications

- Isolation voltage:
 - 1500 VAC
- Supply voltage/power consumption:
 - +5V (-3%/+5%), tbd
 - +3.3V (-5%/+5%), tbd

Mechanical Specifications

- Dimensions: conforming to IEEE 1386.1
- Weight: 78g

Environmental Specifications

- Temperature range (operation):
 - -40..+85°C (qualified components)
 - Airflow: min. 1.0m/s
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 1g/10..150Hz
- Conformal coating on request

MTBF

- tbd @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

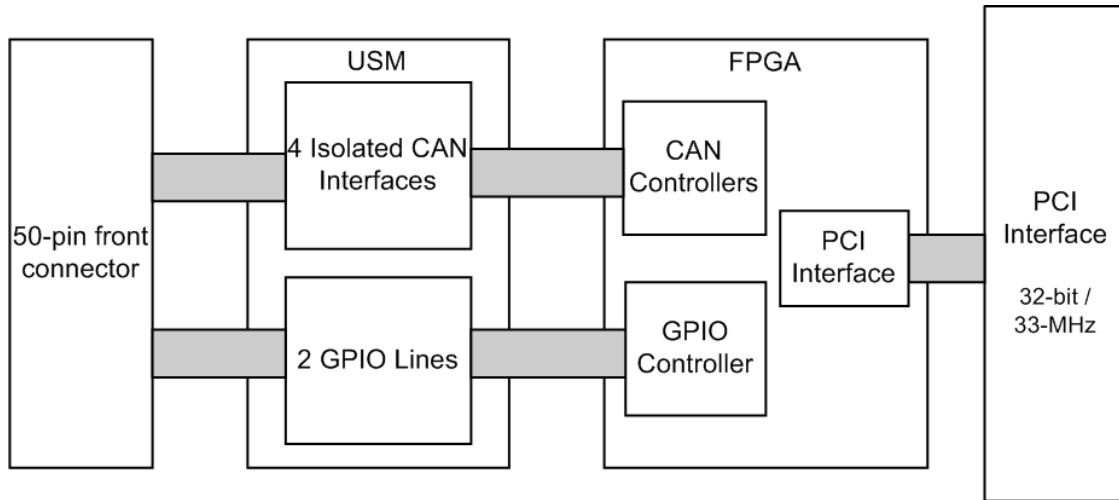
EMC

- Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support

- Windows® (in preparation)
- Linux (in preparation)
- For more information on supported operating system versions and drivers see Software.

Diagram



Configuration & Options

Standard Configurations

Article No.	Main FPGA Content	Soft Core	Memory	Signals	Cooling Method	Operation Temperature
15P506-00	4 CAN bus interfaces	No	32 MB RAM, 2 MB Flash	Front	Convection	-40..+85°C

Options

CPU

- Nios® soft core implementation possible (e.g. for real-time Ethernet)

Rear I/O

- Via Pn4 rear I/O connector

Cooling

- Conduction Cooling

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- [You can find more information on our web page "User I/O in FPGA"](#)

FPGA Capabilities

- FPGA Altera® Cyclone® II EP2C35
 - 33,216 logic elements
 - 483,840 total RAM bits
 - Supports Nios® II soft processor
- Connection
 - Functions can be linked to Wishbone or Avalon® bus
 - Available pin count: 46 pins (FPGA to USM™)
 - Functions available via USM™ at front I/O connector
- [MEN offers a USM™ development kit and an FPGA Development Package as well as Flash update tools for different operating systems.](#)

Ordering Information

Standard Hardware

15P506-00 Quad CAN bus interface, 4 CAN cores, front I/O, for convection cooled systems, -40..+85°C with qualified components

Software: OS independent

13Z015-06 MDIS4/2004 driver (MEN) for 16Z029_CAN (MSCAN/Layer2)

13Z016-06 MDIS4/2004 driver (MEN) for 16Z029_CAN (CANopen master)

13Z061-06 MDIS4/2004 low-level driver sources (MEN) for 16Z061_PWM

Software: Windows

13Z016-70 MDIS4/2004 Windows driver (MEN) for 16Z029_CAN (CANopen master)

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the P506 online data sheet under » www.men.de.

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