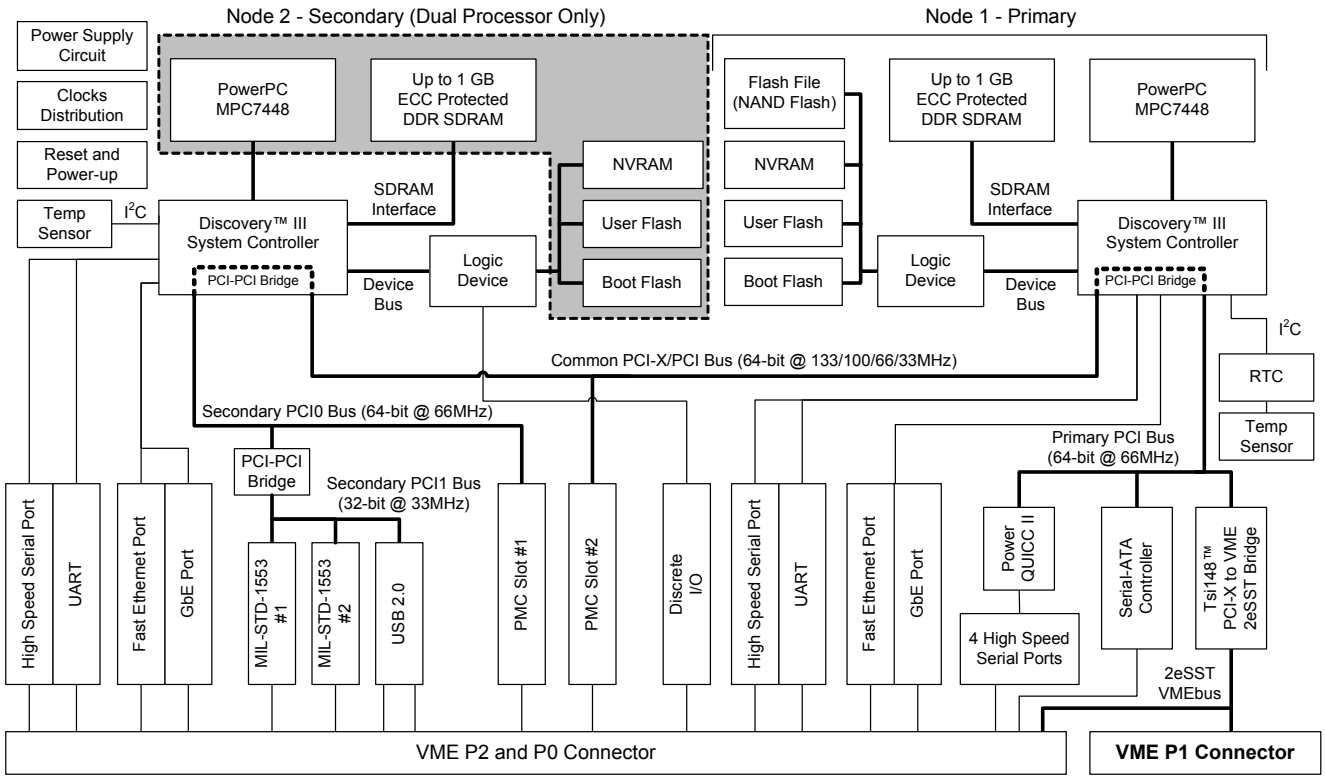
C102

Dual PowerPC® 7448 VME SBC

- Rugged 6U VME Single–Slot SBC
- Dual/Single PowerPC® G4+
  - MPC7448 @ up to 1.42 GHz
  - On-chip 32 kB L1 + 1 MB L2 Cache
- Up to 2 GB Total DDR SDRAM with ECC
- 512 MB Total User Flash
- 256 MB Total Boot Flash
- 256 kB Total NVRAM
- Up to 16 GB Flash File (NAND Flash) Memory for Mass Storage
- VME 2eSST with Legacy VME Support
- Two Gbit Ethernet Ports (10/100/1000)
- Two Fast Ethernet Ports (10/100)
- One Serial ATA II Port (3.0 Gbps)
- Two USB 2.0 Ports (400+ Mbps)
- Two Dual Redundant MIL-STD-1553B Ports
- Six Multi-Protocol High-Speed Serial USART Ports - RS-232/422/485
- Two Standard Serial UART Ports - RS-232/422/485
- 16 Single Ended TTL/8 Differential RS-422 Discrete I/O Lines
- Two PMC Slots
- Eight 32-bit Timers (4 per processor) + Watchdog Timer
- Real Time Clock
- RTOS Support – VxWorks®, Integrity®, LynxOS® and more…
- Extended Temperature: Conduction- and Air-Cooled Versions
- Vibration and Shock Resistant

Aitech Defense Systems, Inc.
A member of the Ai-Rugged Group
9301 Oakdale Ave, Chatsworth, Ca 91311
Tel: (888) Aitech-8 (248-3248) Fax: (818) 718-9787 e-mail: sales@rugged.com web: www.rugged.com



C102 Block Diagram

C102 – Double the Performance, Expanding the I/O

The C102 is a fully loaded Dual/Single PowerPC® 7448, single slot VME SBC specifically designed to endure harsh environment applications. With its distributed architecture, the C102 provides two independent, high performance processing nodes each supported by its own extensive on-board memory resources, communicating with each other over a high speed PCI interconnecting bus. Complementing these powerful processing nodes, the C102 provides the industry's highest functional density feature set of memory and I/O interfaces, which positions the C102 as the best SBC in its class due to the unique combination of processing power and I/O resources.

The C102 is backward compatible with Aitech's previous generation SBCs – the C100/C101/C103 series (the only exception is the IEEE1394 FireWire ports not available) – thus providing an easy migration path for customers using the C10x family SBC products.

Each of the two C102 fully independent processing nodes are powered by Freescale's advanced PowerPC® G4+ MC7448 microprocessor with its integrated on-chip, high speed L1 and L2 caches. The two independent processing nodes employ two separate Discovery™ III System Controllers. Each processing node includes dedicated memory resources designed to take full advantage of the MC7448 processing power, eliminating bottlenecks in data flow. Memory arrays include large and fast DDR SDRAM memory, Boot Flash for firmware and application storage, User Flash for user application and data storage and NVRAM for user/application specific parameters storage. In addition, the primary processing node includes a high-density Flash File (NAND Flash) for mass storage purposes.

The C102 further expands the unparalleled I/O capabilities provided in the former C10x series boards. Its integrated on-board I/O resources include two Gigabit Ethernet ports, two Fast Ethernet ports, two dual

redundant MIL-STD-1553B interfaces, two USB 2.0 ports, one Serial ATA II channel, eight serial ports (six high-speed ports and two standard UARTs) and up to 16 general-purpose discrete I/O channels.

To complement its extensive capabilities and provide extended resources and flexibility, C102 is equipped with two PMC slots allowing installation of additional modules on the board.

The C102 is VME64x compliant, and supports VME advanced protocols such as 2eSST and 2eVME while maintaining full compliance with legacy VME operation.

The C102 SBC internal interconnecting buses are PCI-X/PCI buses split into four segments, with the PCI agents I/O resources distributed between them according to their PCI operation capabilities. This architecture maintains high operation frequency for the high-speed PCI-X/PCI resources while lower capacity PCI resources are located on slower PCI segments. Most of the C102 PCI-X/PCI resources utilize their integrated DMA engines and take full advantage of the PCI-X/PCI protocol in order to achieve maximum bus utilization.

The C102 mechanical and electrical design guarantees its operation over the full range of rugged applications environments and is available both in industry standard conduction- or air-cooled form factors.

Functional Description

Board Architecture

Distributed Processing

The C102 is a powerful processing SBC designed as a distributed processor platform with two independent processing nodes. Each of the processing nodes is a complete sub-system that includes the processor, its local memory resources and basic I/O interfaces (Ethernet and Serial I/O). Each of the two processing nodes is designed around the Marvell Discovery™ III System Controller, a powerful, highly integrated device providing all interconnection between the processor, memory and internal PCI buses.

The two processing nodes communicate with one another through a high performance 133MHz PCI-X bus. The processing nodes communicate using shared memory regions and inter-processor message passing capabilities integrated in the Discovery™ III System Controller design such as doorbells, hardware semaphores, and mutual interrupting mechanisms in addition to other synchronization methodologies.

The C102 SBC may also be configured as a single processor board for power sensitive or less demanding applications. When configured as a single processor SBC the secondary processor and memory array resources are not populated.

Any of the SBC I/O resources may be mapped to either one of the two processing nodes allowing the distribution of the application elements and I/O handling between the two processors. This allows the user to balance the processing loads between them and achieve the highest possible performance.

Processor

The C102 features two high performance G4+ MC7448 PowerPC® processors. The MPC7448 is a 64-bit RISC processor integrating both L1 (32kB instruction/data) and L2 (1MB) caches on chip to support its powerful processing core.

The MC7448 Processor operates at up to 1.42 GHz (with higher frequency processors available in the future) and provides AltiVec support, thus allowing the user to take full advantage of the processor's powerful vector processing capabilities.

System Controller

The C102 implements two MV64460 Discovery™ III System Controllers, one per node, supporting the processing node's high performance and providing a fast highway for high throughput data transfers.

The highly integrated Discovery™ III system controller performs both as the memory controller for the processor and as its interconnecting bridge to the PCI domains.

Each Discovery III System Controller is configured to support the processors MPX bus protocols at 166/133 MHz, and provides two separate and totally independent PCI-X/PCI bus interfaces. Both PCI-X/PCI buses support 64-bit operation at up to 133/100/66/33 MHz and fully comply with PCI Rev. 2.2 and PCI-X Rev. 1.0 specifications.

PCI Bus Segmentation

The C102 bus architecture maximizes PCI bus utilization by employing PCI bus segmentation. The C102 includes several PCI bus domains each configured with its specific operation capabilities with regard to bus frequency and width. High-speed PCI agents requiring high data bandwidth are separated from slower agents that reduce the bus operation capabilities.

The four PCI bus segments are as follows:

- Common PCI bus – interconnecting the two Discovery™ III System Controllers allowing for high-speed communication between the two processing nodes. This segment also includes PMC slot 2. The on-board logic is designed to detect the presence of a PMC and adjust the PCI operation mode and speed according to the PMC capabilities (this is done through the PCIXCAP and M66EN signals). With no PMC installed this segment will utilize 64-bit PCI-X at 133 MHz. If a PMC is installed that supports PCI-X the bus speed will be reduced to 100 MHz. If a PMC is installed that does not support PCI-X the bus segment will be set to PCI operation at the frequency supported by the PMC – 66 MHz or 33 MHz.
- Primary PCI bus: connecting to the primary processing node's System Controller. This is a 64-bit PCI bus operating at 66 MHz. The segment hosts the on-board high-speed elements – PowerQUICC II, Serial ATA II controller, and Tsi148 VME 2eSST Bridge.
- Secondary PCI bus 0: connecting to the secondary processing node System Controller. This bus hosts PMC slot 1 and a PCI-PCI Bridge connecting to Secondary PCI bus 1, hosting lower speed PCI agents. With no PMC installed this bus operates as 64-bit PCI at 66 MHz. If a PMC is installed the bus segment operation speed will be set by the PMC capabilities – 66 MHz or 33MHz.
- Secondary PCI bus 1: connecting to the PCI-PCI Bridge residing on secondary PCI bus 0. This bus segment hosts all the on-board slow PCI agents – USB 2.0 controller and two MIL-STD-1553B controllers. This bus employs 32-bit PCI bus at 33 MHz.

Interrupt Mechanism

To allow for maximum flexibility and further support the capability of each of the two processors to handle any of the SBC's I/O resources the C102 implements a unique interrupt mechanism allowing the routing of each of the on-board resources to any of the two processors.

Memory

The C102 is equipped with large memory arrays providing the user with extensive resources. These arrays are distributed between the two processing nodes and are similar for both nodes with the exception of the Flash File (NAND Flash array). The memory resources supporting each of the processing nodes include up to 1 GB fast DDR SDRAM operating at 166 MHz, 128 MB linear Boot Flash, 256 MB linear User Flash and 128 kB NVRAM (Non-Volatile RAM).

Boot Flash is used for Aitech proprietary firmware storage as well as user application storage. User Flash is intended for user application and data storage. NVRAM can be used for application specific parameters storage and logging purposes.

The Boot Flash area containing Aitech firmware is locked and unavailable to the user. It is protected through a hardware jumper for programming and cannot be altered during normal operation of the board.

The NVRAM technology is fast Flash shadow type of RAM and does not require an external power supply to maintain its contents during power down. It includes Auto-store capability, automatic storage of the RAM contents upon detection of a power down event, ensuring no data is lost when power is cycled off.

In addition to the above memory elements the C102 includes up to 16 GB Flash File (NAND Flash) for solid-state mass storage applications. Double size Flash file is available as a special option - please contact your Aitech sales representative.

The DDR SDRAM arrays are ECC protected guarantying high data integrity.

VME

The C102 implements Tundra's Tsi148 PCI-X to VME 2eSST Bridge for interconnection to the VME bus. The VME Bridge is located on the primary fast PCI bus allowing for high-speed operation and throughput.

The VME interface provides full master and slave capabilities and supports the following:

- 2eSST and 2eVME protocol support
- Legacy traditional VME protocol support
- A64/A32/A24/A16 addressing modes
- MBLT/BLT/D64/D32/D16/D8 data transfer modes
- Interrupter and handler capability on all seven VME interrupt lines
- Four mailbox and four location monitors for in-system board communication
- Full system controller functionality – arbitration, VME clock generation, VME global timeout timer (BERR)
- Flexible register set allowing manipulation of all VME options

The Tsi148 Bridge incorporates large FIFOs for optimal usage of the two buses on which it operates (PCI and VME). In addition, it includes two DMA engines supporting high data rate transfers.

I/O Interfaces

Complementing its superior processing power and on top of the traditional serial I/O capabilities such as Ethernet and serial communication, the C102 also offers advanced serial I/O interfaces such as Serial ATA II and USB. These interfaces allow attachment of advanced fast peripherals and storage devices as well as pointing devices and other USB or SATA peripherals.

Ethernet

The C102 provides four Ethernet ports, Two Gigabit Ethernet and two Fast Ethernet ports. The GbE ports support 10BaseT/100BaseTX/1000BaseT while the Fast Ethernet ports support 10BaseT/100BaseTx.

All four Ethernet MACs are integrated in the Discovery™ III System Controller and utilize dedicated SDMA (Serial DMA) engines to support their operation. Coupled with the Discovery™ III internal SRAM elements the ports are capable of high communication rates.

The C102 in its dual processor configuration assigns two Ethernet ports (one GbE and one Fast Ethernet) to each one of the two processing nodes. In the single processor configuration the primary processor controls the secondary Discovery™ III ports over the common PCI-X/PCI bus.

Serial I/O

The C102 provides eight serial ports supporting RS-232/422/485 physical interfaces.

Six of these channels are high-speed multi-protocol synchronous/asynchronous ports supporting all common serial communications protocols (UART, USART, SDLC, HDLC, BISYNC, Transparent, etc.)

The remaining two serial ports implement standard asynchronous UART-based ports.

Four of the high-speed multi-protocol serial channels are implemented using a PowerQUICC II communication processor. The PowerQUICC II resides on the primary fast PCI bus allowing high-speed operation and high throughput of the serial channels. Each of the PowerQUICC II serial channels is controlled through a dedicated controller each containing its SDMA (Serial DMA) engine and operating with minimal host processor intervention.

Four other serial channels are integrated in the Discovery™ III System Controller, two per node. Two of the channels are high-speed multi-protocol interfaces and two are simple UART ports.

In its dual processor configuration, the C102 assigns two serial ports (one high-speed and one UART) to each of the two processing nodes. In the single processor configuration the primary processor controls the secondary Discovery™ III ports over the common PCI-X/PCI bus.

Serial ATA II

The C102 provides one Serial ATA II channel implemented with a Silicon Image's SIL 3124 PCI-X to SATA II Controller. The controller integrates in it both the SATA link and PHY. The controller is fully compliant with the SATA 1.0 specification and the SATA II extensions, capable of 3.0 Gbps SATA II operation. The controller also integrates two DMA engines and advanced SRAM elements to enhance its operation and achieve high bandwidth when communicating between the local PCI bus and the external mass-storage devices. The SATA controller is located on the primary fast PCI bus allowing for high-speed operation and throughput.

USB 2.0

The USB protocol is a widely used interface and is fully supported by the C102. The board includes a USB host controller – ISP1562 by Philips, providing two EHCI/OHCI ports each supporting USB 2.0 with backward compatibility to Rev. 1.0 and Rev. 1.1. The controller integrates the USB transceivers supporting high-speed, full-speed and low-speed signaling and provides power to down stream devices over the USB interface. The controller is a PCI device capable of high data transfer rates through the use of its internal FIFOs and DMA engines.

The USB controller support 33MHz PCI operation and therefore resides on the slower secondary PCI bus segment.

MIL-STD-1553B

The C102 provides two on board dual redundant MIL-STD-1553B ports. These ports are implemented using two separate PCI controllers – BU-65864 by DDC. Each of the controllers is capable of BC, RT and MT operation.

The MIL-STD-1553B controllers support 33 MHz PCI operation and therefore are located on the slower secondary PCI bus segment.

Discrete I/O

The C102 is equipped with up to 16 single-ended or 8 differential general-purpose Discrete I/O channels. The Discrete I/O controller is integrated in one of the C102 logic elements. The channels can be independently set for single-ended TTL operation or as pairs for differential RS-422 operation. Each of the channels can be independently configured as input or output. Configured as input each of these channels may be programmed to generate an interrupt on any level shift event.

PMC I/O Expansion

The C102 provides two IEEE 1386-2001 or ANSI/VITA 20-2001 compliant PMC expansion slots for extended flexibility and integration of additional I/O to the board.

Each of the PMC slots resides on a different PCI bus segment. PMC slot 1 is located on the secondary PCI bus supporting 64-bit at 33/66 MHz bus operation. PMC slot 2 is located on the common PCI bus, which is the fastest PCI bus segment available on the C102, supporting 64-bit PCI-X at 133/100MHz and PCI at 33/66 MHz bus operation. For both PMC slots the PMC installed will determine the bus operating frequency of all other PCI resources located on the corresponding PCI bus segment. The C102 provides support for the full PCI operation capabilities.

Both PMC slots are capable of hosting IEEE1386/ 1386.1-2001 compliant air-cooled and VITA 20-2001 compliant conduction-cooled PMC modules.

Both PMC slots are universal slots, capable of hosting PMCs with either 3.3V or 5.0V PCI signaling levels. All of the C102 on-board PCI resources are 3.3V devices with 5.0V tolerance. The keying for both slots is universal (no key).

I/O Routing

All I/O interfaces signals are available at the C102 P2 and P0 VME backplane connectors.

The C102 provides full backward compatibility with the previous generation C100/C101/C103 SBCs with relation to the I/O pins mapping at the VME connectors.

Since the I/O interfaces require more I/O pins than is available at the VME connectors, the C102 is available in several different I/O configurations.

The two primary configurations are on-board I/O routing to the VME connectors and PMC I/O routing to VME connectors per VITA 35-2000.

For more information please contact an Aitech Systems representative.

Air-cooled versions of the C102 provide some of the I/O interfaces at the front panel. Refer to the front panel section for more information.

Transition Module

For convenient connection to the C102 I/O interfaces a transition module is available from Aitech.

The TM102 transition module provides accessibility to all C102 I/O interfaces with industry standard connectors, eliminating the need for any custom made harnessing and complex cabling fixtures.

It also provides easy access to PMC I/O for PMC cards installed on the C102. The TM102 may be installed into air-cooled chassis supporting both front and rear plug-in units or front plug-in units only.

For more information on the TM102, refer to its product datasheet.

Timers

Each of the two processing nodes of the C102 is equipped with four 32-bit timers/counters. These timers provide high-resolution timing functionality as well as capability for long interval counting applications.

The C102 includes a Real-Time Clock (RTC) located at the primary node for time and date storage. The RTC is backed up by a large super-capacitor for long-term parameters storage.

The C102 provides two user programmable watchdog timers. The first is a standard timer, which will generate a timeout event when not toggled before the programmed time interval expires. The second timer is a windowed watchdog timer, which requires the timer toggling to be performed within a specific “window” of time. This means that if the timer is toggled before or after the programmed time “window” it will generate a timeout event. Each of the two timers may be independently set to generate a non-maskable interrupt or reset the SBC.

Front Panel Connectors and Switches

The air-cooled version of the C102 SBC is provided with a front panel. The front panel includes the following:

- D-Type connector delivering 2 UART ports (one per node)
- Two RJ-45 jacks providing two Fast Ethernet port (one per node)
- Reset Switch

Software

Test and Diagnostic Features

The C102 is supplied with an extensive firmware package. This package includes startup firmware (boot software), AIMon monitor/debugger tool, AIDiag diagnostic tool, and BIT. BIT may be executed during power-up or at any time after the board has been booted.

The C102 provides a COP/JTAG interface for each of the two processing nodes processors for debugging and development purposes.

RTOS Support

A BSP (Board Support Package) for the C102 is available for several RTOS (Real-Time Operating Systems), including WindRiver VxWorks 5.5 and VxWorks 6.x, Green Hills INTEGRITY®, and LynxOS®.

Other RTOS BSP may be available upon request.

The BSP includes drivers for all on board resources including inter-processor communication capabilities allowing the user to take full advantage of the board’s powerful features.

Mechanical Features

The C102 is available in two mechanical formats:

- Air-cooled per ANSI/VITA 1-1994
- Conduction cooled per IEEE 1101.2

Both mechanical formats are single slot 6U modules.

Custom metal frame provides excellent rigidity and shock resistance. In addition, a custom metal frame provides an array of stiffeners to support rugged PMC boards.

Dimensions

- Air-cooled: per ANSI/VITA 1-1994
- Conduction cooled: per IEEE 1101.2

Weight

Air-cooled form factor: < 800 g (1.75 lbs)

Conduction-cooled form factor: < 900 g (2.0 lbs)

Mechanical Design & Thermal Management

The C102 employs a sophisticated and advanced mechanical design based on years of experience. The mechanical design allows for optimal heat conduction across the C102 and relief of the SBC for both convection and conduction mechanical formats. This mechanical design also ensures the C102 rigidity and endurance under extreme environmental conditions.

C102 Air-Cooled

The air-cooled rugged C102 VME board fully complies with ANSI/VITA 1-1994. This includes a reinforced front panel, and add-on 3D monolithic finned heatsink/ rugged stiffening frame for improved thermal and mechanical properties.

The two air-cooled PMC sites are ready for installation of commercial and rugged air-cooled PMCs that comply with IEEE STD 1386-2001.

The front panel is equipped with two insertion/extraction handles suitable for the VME64x forces, and with openings for the two PMC front panels. The board is shipped with easily removable filler panels in the PMC front panel openings.

C102 Conduction-Cooled

The conduction-cooled rugged C102 VME board fully complies with IEEE 1101.2. It includes a thick 3D monolithic hard anodized aluminum heatsink plate, with built-in stiffening ribs. The geometry of the heatsink ensures efficient heat conduction to the side rails. Wedgelocks attached to the heatsink hold the board firmly in place and ensure good thermal contact to the chassis for effective heat rejection from the board. This mechanical structure is extremely durable and particularly suitable high power BGA and SMT components mounted on the top layer of the board. The low profile SMT components on the bottom side dissipate their heat by additional flat plate conducting the heat to the sides as well. This structure creates also a closed faraday cage structure, excellent for EMI/RFI, RE and RS protection. The heatsink also features board extractors to facilitate removal of the board from it's enclosure.

Two sites for conduction-cooled rugged PMCs meet the ANSI/VITA 20-2001 standard for assembly on the board. The PMC sites utilize a conduction path to the aluminum heatsink to transfer their heat to the carrier board's heat sink. There are two removable ribs providing an additional heat transfer path for PMCs having a secondary thermal interface. For boards with only a primary thermal interface, these ribs can be easily removed.

The conduction-cooled board contains no front panel and all PMC I/O signals are directed to the P2 and P0 I/O connectors of the board.

The C102 was thermally designed to provide high efficiency heat conduction between the high power CPUs to the side rails. The two edges of the PCB are cut so the single piece heatsink is in direct contacting with the chassis sidewall rails without the interface of the PCB. The two processors are mounted with their on board power supplies near the edges of the board. All other heat generating sources are located so to create the shortest yet symmetrical heat path, thus the heat is equally dissipated to both sides of the board.

Power Requirements

The C102 takes all its power from the VME64x backplane. It should be provided with +5.0V, +3.3V and ±12V as defined by the VME64x specification (±12V are required for PMC compliance only, the C102 does not require ±12V for its own operation).

All other power sources required by C102 resources are generated on board.

Total power consumption of the C102 depends on its configuration and assembly options.

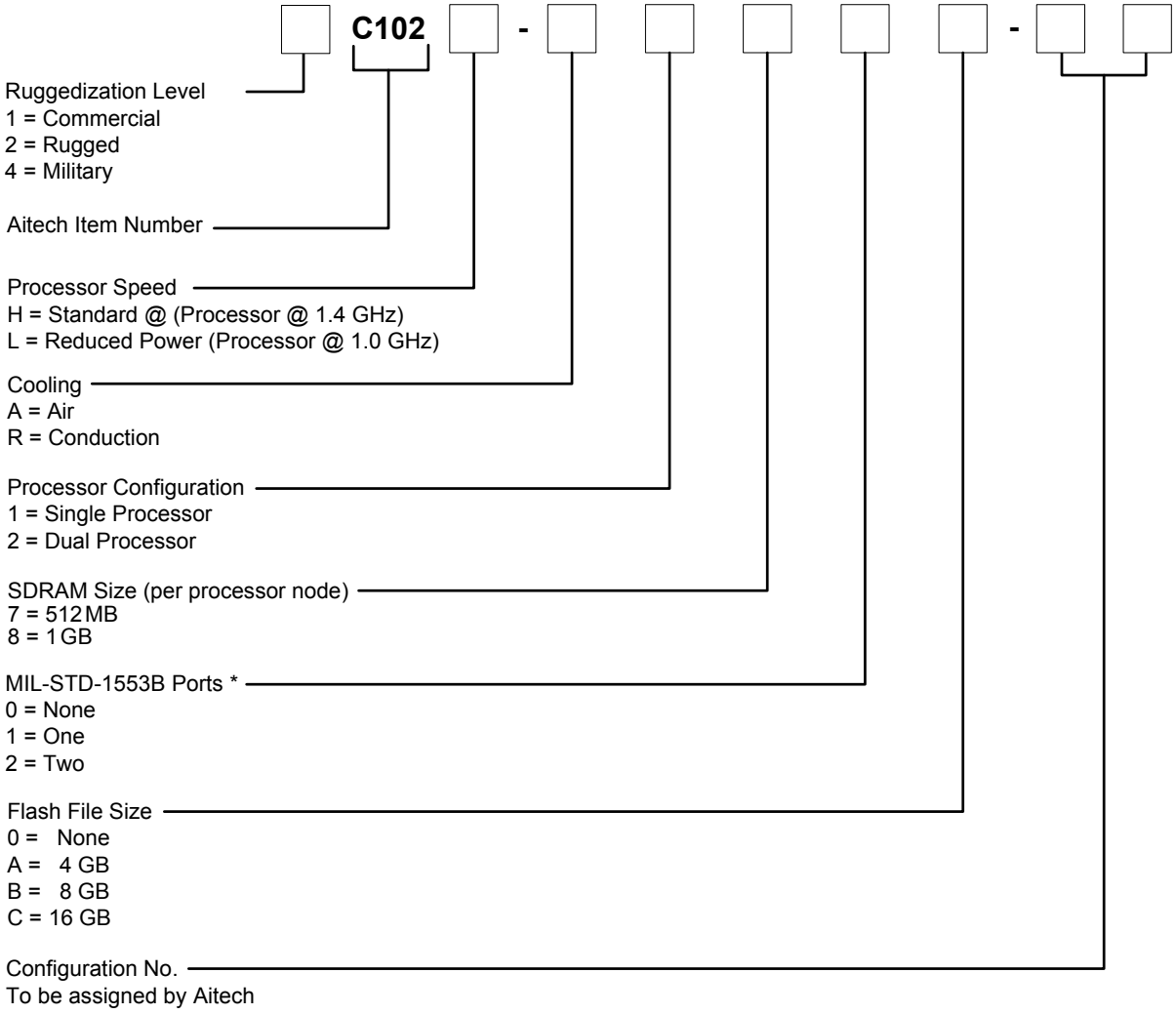
Fully featured, dual processor configuration, C102 power consumption is approximately 40 W, as follows:

+3.3 V	(± 5%)	3.8 A (nominal)
+5.0 V	(± 5%)	5.4 A (nominal)
+12 V	(± 10%)	0 A (no PMC mounted)
–12 V	(± 10%)	0 A (no PMC mounted)

Environmental Features

Please Refer to the Aitech Ruggedization Datasheet.

Ordering Information for the C102



Example: 4C102L-R272B-00

* Default configuration of MIL-STD-1553B controllers is transformer coupled. Direct coupling is optionally available.

Diamond Point International (Europe) Ltd
Suite 13, Ashford House, Beaufort Court
Sir Thomas Longley Road, Rochester, Kent, ME2 4FA, UK
Phone 01634 300900 - Fax 01634 722398 - Email sales@dpie.com – Web www.dpie.com

Aitech Defense Systems, Inc.
A member of the Ai-Rugged Group
9301 Oakdale Ave, Chatsworth, Ca 91311
Tel: (888) Aitech-8 (248-3248) Fax: (818) 718-9787 e-mail: sales@rugged.com web: www.rugged.com