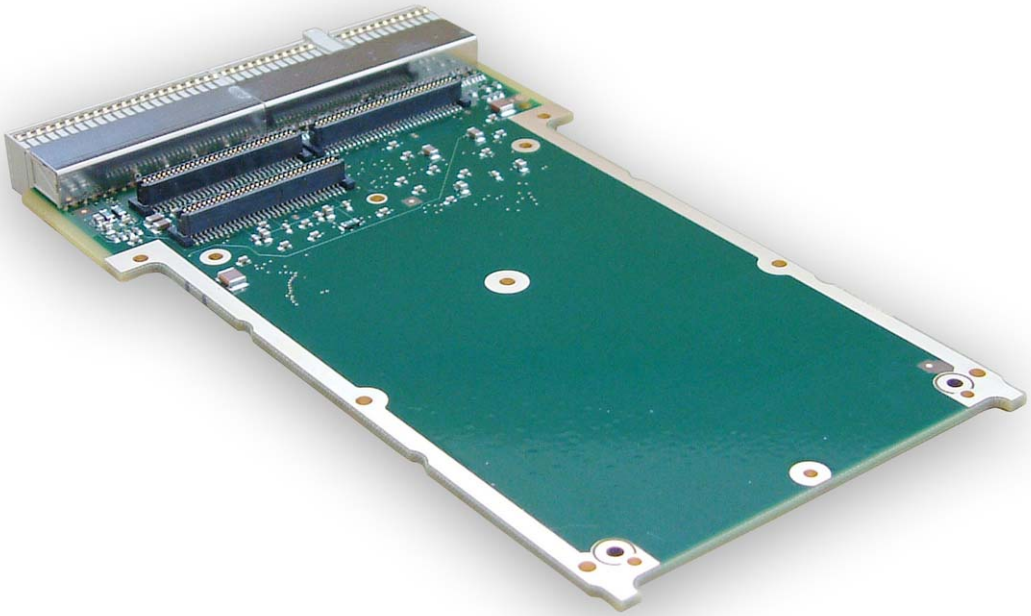

CPMC1 Board
3U cPCI PMC Carrier
User's Guide

CA.DT.A46-1e — April 2009

kontron

Revision History

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

Personal Injury

Be careful while handling the board, because of the cutting edges of the CPU heatsink.

Do not touch the CPU heatsink or the ruggedizer while removing the board from a rack because it can get very hot.

Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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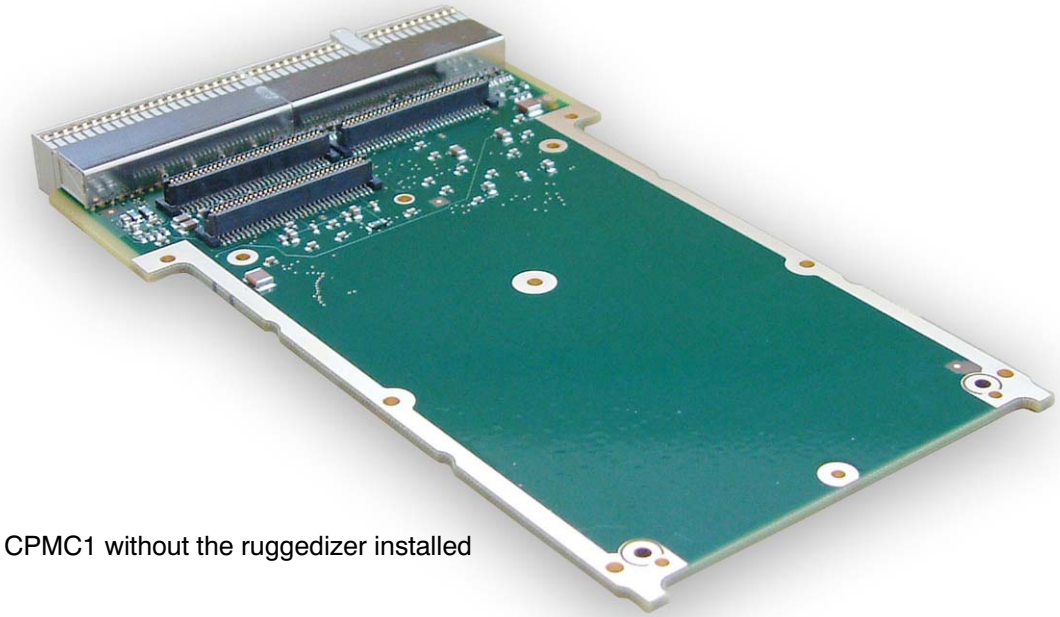
Chapter 1 - Overview

The CPMC1 is a standard 3U CompactPCI carrier that provides rear I/O for a single width rugged conduction-cooled PMC module.



CPMC1 without the ruggedizer installed

Figure 1: CPMC1 Overview

1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the CPMC1 carrier board.

> Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.2 Audience

This manual is a guide and reference handbook for engineers and system integrators who wish to use Kontron' CPMC1 carrier board. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding, Compact PCI, and communications. There is a glossary provided at the back of this guide that explains some of the terms used and expands all abbreviations.

1.3 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 (this chapter) - Brief introduction, this guide's objectives and audience, the structure, some warnings, conventions, and related documentation.
- Chapter 2 - Technical Specification
- Chapter 3 - Preparing before Using
- Chapter 4 - Functional Description
- Chapter 5 - Connectors

1.4 Conventions


This symbol indicates an Electrostatic Sensitive Device (ESD)


To reduce the risk of personal injury and/or equipment damage, follow the instructions

This symbol indicates general information

- All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.
- The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

- Signal names ending with an asterisk (*) denote active low signals; all other signals are active high.
- Following the PCI convention, signal names ending with a # denote active low signals; all other signals are active high.

1.5 Related Documents

Hardware

- PowerEngineC7 Single PowerPC 750FX - User's Guide CA.DT.A31
- CP3210 Single PowerPC 750FX - User's Guide CA.DT.A57

Chapter 2 - Technical Specification

Order Code

CPMC1-RC-000	cPCI Carrier Board

Technical Specification

CompactPCI Interface	CompactPCI 3U, conforming to PICMG 2.0 R3.0
PCI Interface	PCI 2.2 compliant interface, 33 MHz, 32 bits
PCI I/O Signaling Voltage	Standard: 3.3V Optional: 5.0V; please contact Kontron
PMC Slots	1
I/O Access	P14 I/O via P2/J2
Power Requirements without PMC Module	10 mA typical @ VI/O DC Additional power is required by the PMC module
Temperature Range	Operating: -40°C to + 85°C Storage: -45°C to +100°C
Weight	205 g
Size	160 x 100 mm
Humidity	5-95 % without condensation

Table 1: Technical Specification

MTBF Data

Calculations are made according to the standard MIL HDBK 217F Notice 2.

Results below are given for four types of environment:

- Ground Benign GB
- Air Inhabited Cargo AIC
- Naval Sheltered NS
- Air Rotary Wing ARW

Ground Benign (Hours)		Air-Inhabited Cargo (Hours)	Naval Sheltered (Hours)		Air Rotary Wing (Hours)
25°C	40°C	40°C	25°C	40°C	55°C
2,872,835	2,255,390	624,521	568,189	445,468	92,365

Chapter 3 - Preparing Before Using

This chapter gives guidelines on preventing static electricity discharge, environmental protection, unpacking, inspecting and identifying the CPMC1.

3.1 Preventing Static Electricity Discharge

During unpacking and installation of the board, it is important to follow proper procedure:

1. To avoid ESD damage don't remove the board from its antistatic packaging without wearing an antistatic wrist strap. Place the strap around your wrist and connect it to an electrical ground. An electrical ground can be a piece of metal that literally runs into the ground (such as an unpainted metal pipe) or a metal part of a grounded electrical appliance. An appliance is grounded if it has a three-prong plug and is plugged into a three-prong grounded outlet.
2. After removing the board from its protective packaging (or chassis), place the board flat on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
3. Store or ship the board into its shipping box, because it is treated to assure an antistatic protection and to be stored in a protected area (EPA).

The antistatic bag is more appropriate for a one-time use and should not be considered for repeated use.

3.2 Environmental Protection

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

3.3 Unpacking

Don't throw out the shipping box, it should be used to store or ship the board.

The CPMC1 is shipped in an individual, reusable shipping box closed by an ESD stick-on label.

1. First, when you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent is present when the carton is opened. Keep the contents and packing materials for the agent's inspection and notify Kontron's customer service department of the incident. Retain the packing list for reference.
2. Assuming that you wear an antistatic wrist strap, you can open the shipping box by cutting the ESD stick label. If the label has already been cutting, please notify the carrier and Kontron immediately.
3. If your box contains foams, remove the first foam. Kontron board is protected by an antistatic envelope.
4. When unpacking the board, observe antistatic precautions (refer to section 3.1 page 5).
5. Closely inspect the board for any signs of shipment-related damages such as loose components or bent pins. If any evidence of damage is discovered, please notify the carrier and Kontron immediately.
6. Work at an approved antistatic workstation and a grounded bench mat.

This package has been designed for shipping and it is not suitable for long-term storage (upper than two years) nor storage under severe conditions. For more information, please contact your Kontron representative.

3.4 Inspection

Assuming that the CPMC1 is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Any defects detected should be reported to Kontron.

3.5 Board Identification

Kontron CPMC1 boards are identified by labels fitted to the bottom side.

➤ Labels fitted to the bottom side of the CPMC1

A "Chronological serial number" label.

B "Variant" and "Engineering Change Level" (E.C. Level) label: The "Variant" number is used with the Self-Tests and manufacturing Self-Tests. In the below example the E.C. Level is **eeee**.

C "Board Idenditification" label (Order Code) of the board.

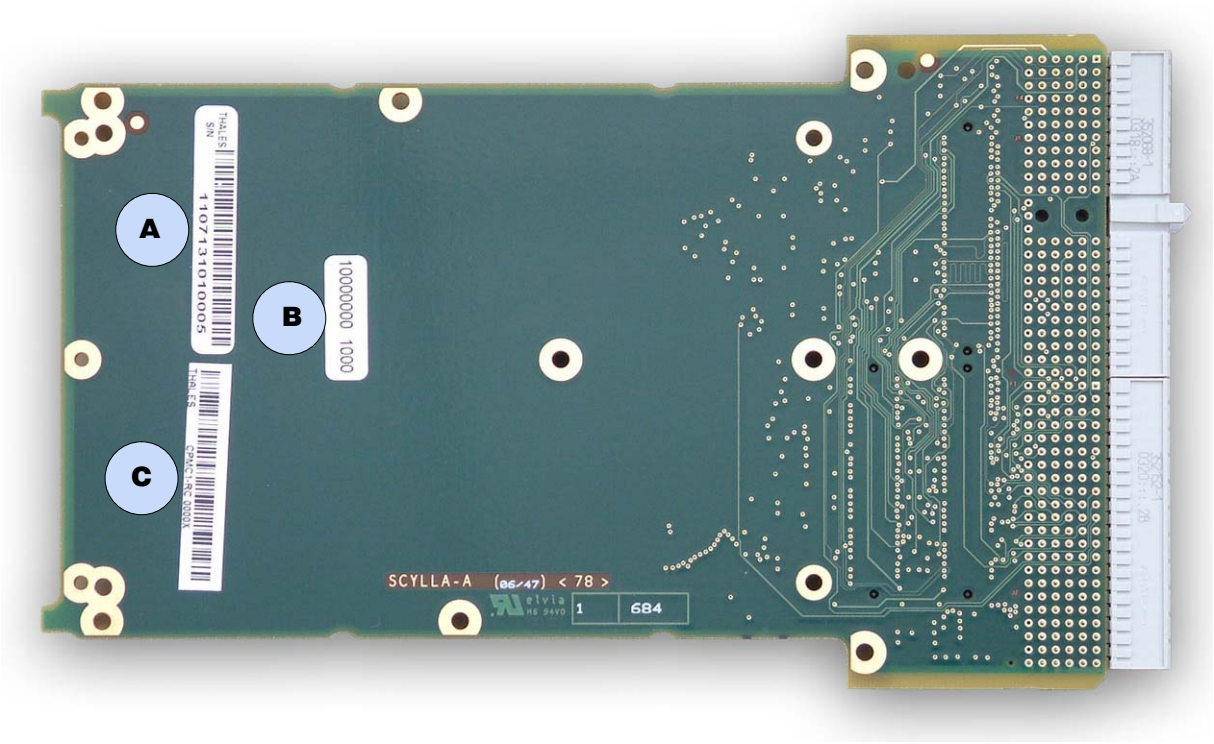


Figure 2: Bottom Side Identification Labels

3.6 Installing or Removing a PMC Module

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

The installation of the PMC on the CPMC1 conforms to the IEEE P1386.1 standard.

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the CPMC1 board or the PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

Take care that your PMC and the PCI environment have the same PCI signaling voltage. If PMC modules are plugged into a PCI environment, and the I/O signaming voltages do not match, damage to the equipment could occur, voiding product warranties.

To install the PMC module, refer to Figure 3 "PMC Installation" and follow the steps below:

1. Place carefully the CPMC1 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Install the PMC, component-side down, aligning the PCI connectors with their mating connectors on the CPMC1. Press them together so that the friction from the pins holds them together.
3. Screw the PMC in place using the 4 mounting points, on the bottom side of the CPMC1 . You need a Phillips screwdriver for this stage.
4. The PMC attachment is now complete.
5. Insert the CPMC1 into the chassis making sure it is properly plugged into the backplane.

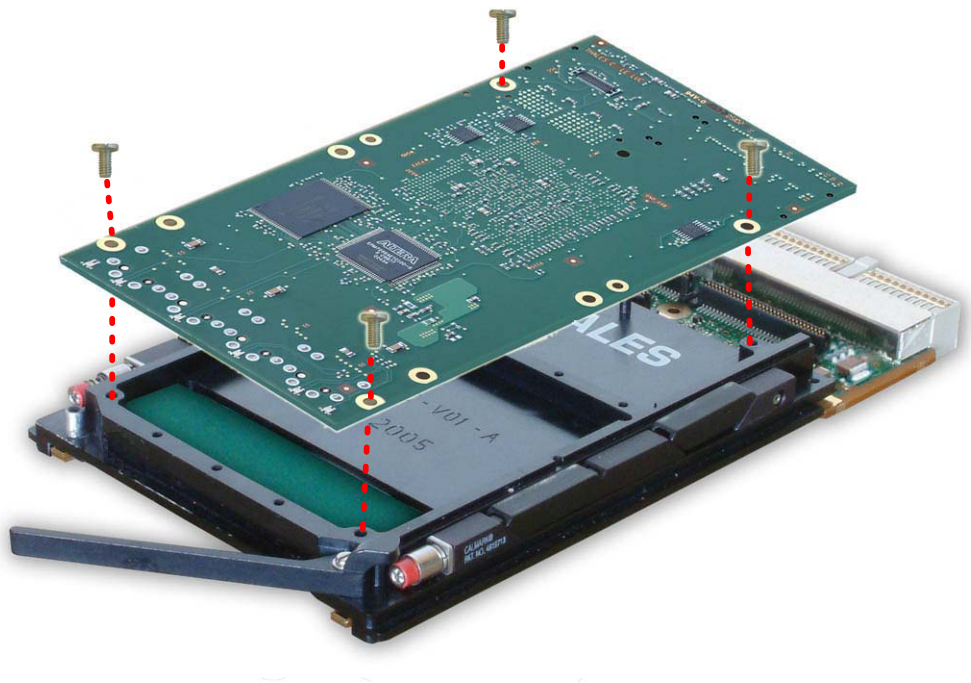


Figure 3: PMC Installation

Chapter 4 - Functional Description

4.1 PMC to PCI Interface

The CPMC1 is a mechanical adaptor to connect a standard PMC module in 3U CompactPCI systems. As such, it is a passive adapter board and has no PCI-to-PCI bridge. The carrier's PCI bus is connected directly to the PMC card's PCI bus.

4.1.1 PCI Signaling Levels and Voltage Keying

As factory default, the CPMC1 is assembled with the 3.3V keying pin. Before mounting a PMC onto the CPMC1, make sure that the PMC and the CompactPCI system have the same signaling voltage.

On the CPMC1, the 3.3V keying pin is interdependent of the ruggedizer and can not be removed.

In the default configuration of a CPMC1, 5V only signaling PMC will not be usable. For more information, please contact your Kontron representative.

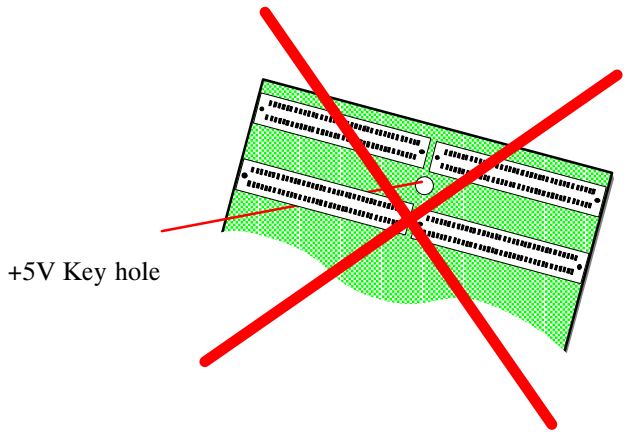


Figure 4: 5V Signaling PMC

Chapter 5 - Connectors

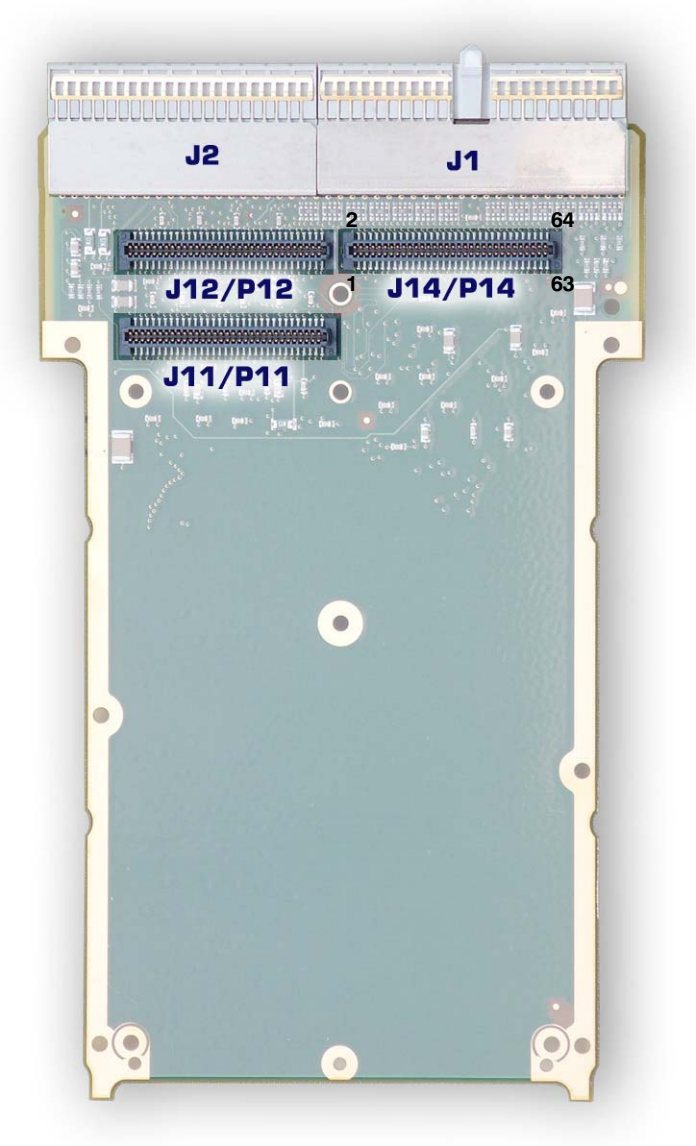


Figure 5: Connectors Location

5.1 CompactPCI J1

Position	Row A	B	C	D	E	F
25	+5V	REQ64#	N.C.	+3.3V	+5V	GND
24	AD[1]	+5V	V(I/O)	AD[0]	ACK64#	GND
23	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	+3.3V	N.C.	N.C.	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	+3.3V	FRAME#	IRDY#	N.C.	TRDY#	GND
12-14	KEY AREA					GND
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	+3.3V	CLK	AD[31]	GND
5	N.C.	N.C.	RST#	GND	GNT#	GND
4	IPMB_PWR	N.C.	V(I/O)	N.C.	N.C.	GND
3	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	TCK	+5V	TMS	TDO	TDI	GND
1	+5V	-12V	TRST#	+12V	+5V	GND

#: Signals active when low.

Table 2: CompactPCI J1 Pin Assignment

For more information about PCI and additional CompactPCI signals, refer to section 5.6 page 17.

5.2 CompactPCI J2

Position	Row					
	A	B	C	D	E	F
22	N.C.	N.C.	N.C.	N.C.	N.C.	GND
21	N.C.	N.C.	N.C.	N.C.	N.C.	GND
20	N.C.	N.C.	N.C.	N.C.	N.C.	GND
19	N.C.	N.C.	N.C.	N.C.	N.C.	GND
18	N.C.	N.C.	N.C.	N.C.	N.C.	GND
17	N.C.	N.C.	N.C.	N.C.	N.C.	GND
16	N.C.	N.C.	N.C.	N.C.	N.C.	GND
15	N.C.	N.C.	N.C.	N.C.	N.C.	GND
14	N.C.	+3.3V	N.C.	N.C.	N.C.	GND
13	PMCIO[05]	PMCIO[04]	PMCIO[03]	PMCIO[02]	PMCIO[01]	GND
12	PMCIO[10]	PMCIO[09]	PMCIO[08]	PMCIO[07]	PMCIO[06]	GND
11	PMCIO[15]	PMCIO[14]	PMCIO[13]	PMCIO[12]	PMCIO[11]	GND
10	PMCIO[20]	PMCIO[19]	PMCIO[18]	PMCIO[17]	PMCIO[16]	GND
9	PMCIO[25]	PMCIO[24]	PMCIO[23]	PMCIO[22]	PMCIO[21]	GND
8	PMCIO[30]	PMCIO[29]	PMCIO[28]	PMCIO[27]	PMCIO[26]	GND
7	PMCIO[35]	PMCIO[34]	PMCIO[33]	PMCIO[32]	PMCIO[31]	GND
6	PMCIO[40]	PMCIO[39]	PMCIO[38]	PMCIO[37]	PMCIO[36]	GND
5	PMCIO[45]	PMCIO[44]	PMCIO[43]	PMCIO[42]	PMCIO[41]	GND
4	PMCIO[50]	PMCIO[49]	PMCIO[48]	PMCIO[47]	PMCIO[46]	GND
3	PMCIO[55]	PMCIO[54]	PMCIO[53]	PMCIO[52]	PMCIO[51]	GND
2	PMCIO[60]	PMCIO[59]	PMCIO[58]	PMCIO[57]	PMCIO[56]	GND
1	N.C.	PMCIO[64]	PMCIO[63]	PMCIO[62]	PMCIO[61]	GND

Table 3: CompactPCI J2 Pin Assignment

For more information about PCI and additional CompactPCI signals, refer to section 5.6 page 17.

5.3 PMC J11 / P11

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	N.C.
11	GND	12	N.C.
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V(I/O)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE[3]#
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	V(I/O)	32	AD[17]
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	N.C.	42	N.C.
43	PAR	44	GND
45	V(I/O)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	+5V
51	GND	52	C/BE[0]#
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	V(I/O)	58	AD[03]
59	AD[02]	60	AD[01]
61	AD[00]	62	+5V
63	GND	64	REQ64#

#: Signals active when low.

Table 4: CompactPCI J11/P11 Pin Assignment

For more information about PCI and additional CompactPCI signals, refer to section 5.6 page 17.

5.4 PMC J12 / P12

Pin	Signal	Pin	Signal
1	+12V	2	TRST#
3	TMS	4	N.C.
5	TDI	6	GND
7	GND	8	N.C.
9	N.C.	10	N.C.
11	BUSMODE2#	12	+3.3V
13	RST#	14	BUSMODE3#
15	+3.3V	16	BUSMODE4#
17	N.C.	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	+3.3V
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE[2]#
33	GND	34	N.C.
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE[1]#	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	+3.3V
51	AD[07]	52	N.C.
53	+3.3V	54	N.C.
55	N.C.	56	GND
57	N.C.	58	N.C.
59	GND	60	N.C.
61	ACK64#	62	+3.3V
63	GND	64	N.C.

#: Signals active when low.

Table 5: CompactPCI J12/P12 Pin Assignment

For more information about PCI and additional CompactPCI signals, refer to section 5.6 page 17.

5.5 PMC J14 / P14

Pin	Signal	Pin	Signal
1	PMCIO[01]	2	PMCIO[02]
3	PMCIO[03]	4	PMCIO[04]
5	PMCIO[05]	6	PMCIO[06]
7	PMCIO[07]	8	PMCIO[08]
9	PMCIO[09]	10	PMCIO[10]
11	PMCIO[11]	12	PMCIO[12]
13	PMCIO[13]	14	PMCIO[14]
15	PMCIO[15]	16	PMCIO[16]
17	PMCIO[17]	18	PMCIO[18]
19	PMCIO[19]	20	PMCIO[20]
21	PMCIO[21]	22	PMCIO[22]
23	PMCIO[23]	24	PMCIO[24]
25	PMCIO[25]	26	PMCIO[26]
27	PMCIO[27]	28	PMCIO[28]
29	PMCIO[29]	30	PMCIO[30]
31	PMCIO[31]	32	PMCIO[32]
33	PMCIO[33]	34	PMCIO[34]
35	PMCIO[35]	36	PMCIO[36]
37	PMCIO[37]	38	PMCIO[38]
39	PMCIO[39]	40	PMCIO[40]
41	PMCIO[41]	42	PMCIO[42]
43	PMCIO[43]	44	PMCIO[44]
45	PMCIO[45]	46	PMCIO[46]
47	PMCIO[47]	48	PMCIO[48]
49	PMCIO[49]	50	PMCIO[50]
51	PMCIO[51]	52	PMCIO[52]
53	PMCIO[53]	54	PMCIO[54]
55	PMCIO[55]	56	PMCIO[56]
57	PMCIO[57]	58	PMCIO[58]
59	PMCIO[59]	60	PMCIO[60]
61	PMCIO[61]	62	PMCIO[62]
63	PMCIO[63]	64	PMCIO[64]

Table 6: CompactPCI J14/P14 Pin Assignment

For more information about PCI and additional CompactPCI signals, refer to section 5.6 page 17.

5.6 PCI and Additional CompactPCI Signal Description

Mnemonic	Description
AD[00] to AD[31]	**Address/Data bits.** Multiplexed address and data bus.
ACK64#	**Acknowledge 64-bit Transfer.** Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	**Bus Mode 1.** Driven low by a PMC module to indicate that it supports the current bus mode.
BUSMODE2# to BUSMODE4#	**Bus Mode**. Driven by the host to indicate the bus mode. Always set to PCI mode on CPMC1.
C/BE[0]# to C/BE[3]#	**Bus Command/Byte Enables**. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus.
CLK	**Clock**. Except RST#, INTA#, INTB#, INTC# and INTD#, all 32-bit PCI bus signals are synchronous to 33 MHz clock.
DEVSEL#	**Device Select**. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	**FRAME**. Driven low by the current master to signal the start and duration of an access.
GNT#	**Grant**. Driven low by the arbiter to grant PCI bus ownership to a PCI agent.
IDSEL	**Initialization Device Select**. Device chip select during configuration cycles.
INTA# to INTD#	**Interrupt lines**. Level-sensitive, active-low interrupt requests.
IPMB_PWR	**System Management Power**.
IRDY#	**Initiator Ready**. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	**LOCK**. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	**66MHZ_ENABLE**. 66 MHz enabling lines is defined as GND for 33 MHz backpanes.
N.C.	This pin is not connected.
PAR	**Parity**. Parity protection bit for AD[0] to AD[31] and C/BE0# to C/BE3#.
PERR#	**Parity Error**. Driven low by a PCI agent to signal a parity error.
PMCIO[01] to PMCIO[64]	**32-bit PCI PMC signals**. Used to transmit I/Os signals from PMC connector (J14) to J2 connector.
REQ#	**Request**. Driven low by a PCI agent to request ownership of the PCI bus.
REQ64#	**Request 64-bit Transfer**. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
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Mnemonic	Description
RST#	**Reset**. Driven low to reset the PCI bus.
SERR#	**System Error**. Driven low by a PCI agent to signal a system error.
STOP#	**STOP**. Driven low by a PCI target to signal a disconnect or target-abort.
TCK	**Test Clock**. Used to clock state information and test data into and out of the device during operation of the TAP (JTAG) controller.
TDI	**Test Data Input**. Used to serially shift test data and test instructions into the device during TAP operation.
TDO	**Test Data Output**. Used to serially shift test data and test instructions out of the device during TAP operation.
TMS	**Test Mode Select**. Used to control the state of the TAP controller in the device.
TRST#	**Test Reset**. Provide an asynchronous initialization of the TAP controller.
TRDY#	**Target Ready**. Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	**PCI I/O Buffer Voltage**. Power supply delivered by the board. Fixed by the backplane.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
-12V	-12 Volts DC power.
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Table 7: PCI and CompactPCI Signal Description

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