DIMM-PC MODULE

Specification

Document Revision 2.1

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2. INTRODUCTION

2.1 DIMM-PC Architecture

The application-specific portion of a standard embedded application typically requires low pin count components such as relays, power supplies and A/D-converters. An embedded PC requires components of much higher pin-count and higher density circuit boards. The DIMM-PC concept separates the high-density circuit board of the embedded PC from the low density, often two-layer, application-specific baseboard.

To simplify the connection of the peripheral components, such as A/D converters, a programmable chip-select-signal has been defined on the DIMM-PC bus. This chip-select-signal can be adjusted in the BIOS setup of the PC for corresponding I/O addresses. With a single external TTL component, up to eight I/O components can be triggered. In the regular ISA bus, the user has to connect 20 pins to a GAL to select an external component. The programmable chip select decodes unnecessary ISA bus address signals. This makes triggering the external bus-buffer components possible.

To address the drawback of a higher price for a PC solution, the DIMM-PC performs without discrete peripheral connectors, significantly reducing the cost. In other PC solutions, such as PC/104, connectors and their assembly are a significant part of the manufacturing costs. In "low end" 386SX-solutions, these costs can be as much as 25%. Because the DIMM-PC performs without connectors, these costs are significantly decreased and the PC can be integrated on a smaller board surface. The reduction in the number of steps necessary in manufacturing and assembling the component group is another cost-decreasing factor.

The two-sided reflow process, as well as exclusion of the wave-solder process, serves to increase the yield in manufacturing and improve quality. The required SO-DIMM connector is a very inexpensive, standard component and is available from numerous manufacturers.

In designing the DIMM PC, attention was directed toward its use in embedded applications. Moreover, its design was developed in co-operation with large-scale customers. Because most peripheral interfaces used in such applications are device-internal (in external interfaces, mainly special customized interfaces are used), the RS232 interface driver components have been excluded from the DIMM-PC, leading the interfaces as pure TTL signals to the outside. This further decreases additional costs, while enabling the user to have more flexibility when selecting the interface driver (RS485, RS422, RS232, TTY etc.) The power consumption of the PC architecture is drastically reduced with integrated components. This makes the system optimally adaptable with power-saving modes.

The PC in the DIMM-PC architecture also has minimized or eliminated some of the most critical disadvantages of the microcontroller:

- The DIMM-PC today needs less board surface than most micro-controller applications.
- The embedded PC cost has been drastically decreased by the DIMM-PC architecture.
- The DIMM-PC architecture has eliminated the complicated cabling of an embedded PC.

The user receives important advantages by using a DIMM-PC. Because of the 100% PC-compatibility, the user can begin the software development immediately on a standard PC. This is a factor that may influence the success of a product in today's market, where "time to market" is of high importance. As target hardware becomes available, it can be implemented with no obstacles to operation because it will be unnecessary to change the software. With the SO-DIMM-connector, an exchange for a more powerful type CPU is possible, increasing the scalability of the ultimate device. In the case of product information and new designs, the CPU may simply be superseded by a new DIMM-PC, saving redesign time. Through continuous development of the DIMM modules, the cost for the life span of a product can be reduced, profiting users. The integrated IDE controller allows the user to work with normal PC tools with no need for hardware-specific drivers.

3. DIMM-PC MODULE PINOUT

3.1 CPU Module Pinout

Pin	Signal	Pin	Signal
1	IOCHCK#	2	GND
3	RSTDRV	4	IDECS0#
5	SD7	6	VCC
7	SD6	8	IDECS1#
9	IRQ9	10	DASP
11	SD5	12	PDIAG/FREI1
13	SD4	14	DTR2#
15	DRQ2	16	RI2#
17	SD3	18	TXD2
19	SD2	20	CTS2#
21	MEMCS16#	22	RXD2
23	SD1	24	RTS2#
25	0WS#	26	DCD2#
27	IOCS16#	28	GND
29	SD0	30	DSR2#
31	SBHE#	32	FDHDSEL#
33	IOCHRDY	34	FDRDATA#
35	IRQ10	36	FDWRPRT#
37	AEN	38	FDTRK0#
39	SMEMW#	40	FDWGATE#
41	IRQ11	42	FDWDATA#
43	SA19	44	FDSTEP#
45	SMEMR#	46	FDDIR#
47	IRQ12	48	FDMTR0#
49	SA18	50	FDDSKCHG
51	IOW#	52	FDDS0#
53	IRQ15	54	FDIDX#
55	SA17	56	USB1-
57	IOR#	58	GND
59	IRQ14	60	SA16
61	DACK0#	62	GND
63	SA15	64	USB1+
65	DRQ0	66	VCC
67	SA14	68	LNLED
69	DACK5#	70	LKLED
71	SA13	72	I2CDAT
73	DRQ5	74	I2CCLK
75	SA12	76	GPCS0#
77	REF#	78	DCD1#
79	SD8	80	DSR1#
81	SA11	82	RXD1

Pin	Signal	Pin	Signal
83	SYSCLK	84	RTS1#
85	SD9	86	TXD1
87	SA10	88	CTS1#
89	IRQ7	90	GND
91	SD10	92	DTR1#
93	SA9	94	RI1#
95	IRQ6	96	STB#
97	SD11	98	AFD#
99	SA8	100	PD0
101	IRQ5	102	ERR#
103	SD12	104	PD1
105	SA7	106	INIT#
107	IRQ4	108	PD2
109	DACK7#	110	SLIN#
111	DRQ7	112	PD3
113	IRQ3	114	PD4
115	SA6	116	PD5
117	SD13	118	PD6
119	DACK2#	120	PD7
121	SA5	122	ACK#
123	SD14	124	BUSY
125	TC	126	PE
127	SA4	128	SLCT#
129	SD15	130	KBDAT
131	BALE	132	KBCLK
133	SA3	134	SPKR
135	MASTER#	136	PGOOD
137	SA2	138	SMISW
139	SA1	140	VCC
141	OSC	142	BATT
143	SA0	144	GND

3.2 I/O Module Pinout

Pin	Signal	Pin	Signal
1	SA0	2	GND
3	OSC	4	BATT
5	SA1	6	VCC
7	SA2	8	RI4#
9	MASTER#	10	DCD4#
11	SA3	12	DTR4#
13	BALE	14	DSR4#
15	SD15	16	RTS4#
17	SA4	18	CTS4#
19	TC	20	TXD4
21	SD14	22	RXD4
23	SA5	24	RI3#
25	DACK#2	26	DCD3#
27	SD13	28	DTR3#
29	SA6	30	DSR3#
31	IRQ3	32	RTS3#
33	DRQ7	34	CTS3#
35	DACk#7	36	TXD3
37	IRQ4	38	RXD3
39	SA7	40	P23
41	SD12	42	P22
43	IRQ5	44	TXD+
45	SA8	46	TXD-
47	SD11	48	RXD+
49	IRQ6	50	RXD-
51	SA9	52	LNLED
53	SD10	54	LKLED
55	IRQ7	56	GND
57	SA10	58	MAD15
59	SD9	60	MAD14
61	SYSCLK	62	MAD13
63	SA11	64	MAD12
65	SD8	66	P21
67	REF#	68	BLUE
69	SA12	70	GREEN
71	I2DAT	72	RED
73	SA13	74	VCC
75	I2CLK	76	VSYNC
77	SA14	78	GND
79	DRQ0	80	HSYNC
81	SA15	82	FPBACK
83	DACK#0	84	P20
85	IRQ14	86	SA16
87	IOR#	88	GND
89	SA17	90	FPVDD
91	IRQ15	92	BLANK#
93	IOW#	94	P15
95	SA18	96	P14

Pin	Signal	Pin	Signal
97	IRQ12	98	P13
99	SMEMR#	100	P12
101	SA19	102	P7
103	IRQ11	104	P6
105	SMEMW#	106	P5
107	AEN	108	P4
109	IRQ10	110	P19
111	IOCHRDY	112	P18
113	SBHE#	114	P11
115	SD0	116	P10
117	IOCS16#	118	GND
119	0WS#	120	P3
121	SD1	122	P2
123	MEMCS16#	124	P1
125	SD2	126	P0
127	SD3	128	P9
129	DRQ2	130	P8
131	SD4	132	VPANEL
133	SD5	134	FPVEE
135	IRQ9	136	VDCLK
137	SD6	138	LLCLK
139	SD7	140	VCC
141	RSTDRV	142	LFS
143	IOCHCK#	144	GND

4. SIGNAL DESCRIPTION

4.1 *ISA Bus Signals*

4.1.1. SD<0..15> (System Data Bus)

Bi-directional I/O pins.

These signals provide data bus bits 0 to 15 for the peripheral devices. All 8-bit devices use SD0 <0..7> for data transfers. The 16-bit devices use SD<0..15>. To support 8-bit devices, the data on SD<8..15> will be gated to SD<0..7> during 8-bit transfers to these devices. The 16-bit CPU cycles will be converted to two, 8-bit cycles for 8-bit peripheral automatically.

4.1.2. SA<19..0> (System Address)

Output from CPU modules.

Input to all other modules.

Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA<17..23>, allow access of up to 16MB of memory. SA<0..19> are gated on the PC/104-bus when BALE is high and latched on falling edge of BALE.

4.1.3. SBHE# (System Bus High Enable)

Output on CPU modules.

Input on all other module.

Bus High Enable indicates a transfer of data on the upper byte of the data bus (SD<8..15>). 16 bit I/O devices use SBHE# to condition data bus buffers tied to SD<8..15>.

4.1.4. BALE (Bus Address Latch Enable)

Output from CPU modules.

Input on any other module.

Bale is an active high pulse, which is generated at the beginning of bus cycles initiated by a CPU module. It indicates when the SA<0..19>, LA<17..23>, AEN, and SBHE# signals are valid.

4.1.5. AEN (Address Enable)

Output from CPU modules.

Input on any other module.

AEN is an active high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.

4.2 *Control Signal Group*

4.2.1. SMEMR# (System Memory Read)

Output from CPU modules.

Input on any other module.

SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active on memory read cycles to addresses below 1MB.

4.2.2. SMEMW# (System Memory Write)

Output from CPU modules.

Input on any other module.

SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active on all memory write cycles to address below 1MB.

4.2.3. IOR# (I/O Read)

Output from CPU modules.

Input on any other module.

I/O read instructs an I/O device to drive its data onto the data bus. The CPU or DMA controller may drive it. IOR# is inactive (high) during refresh cycles.

4.2.4. IOW# (I/O Write)

Output from CPU modules.

Input on any other module.

I/O write instructs an I/O device to store the data present on the data bus. The CPU or DMA controller may drive it. IOW# is inactive (high) during refresh cycles.

4.2.5. IOCHCK# (I/O Channel Check)

Input to CPU modules.

Open collector output on any other module.

IOCHCK# is an active low input signal that indicates an error has taken place on the module bus. If I/O checking is enabled on the CPU module, an IOCHCK# assertion by a peripheral device generates an NMI to the processor.

4.2.6. IOCHRDY (I/O Channel Ready)

Input to CPU modules.

Open collector output on any other module.

The I/O channel ready is pulled low to extend the read or write cycles of any bus access when required. The CPU and DMA controllers or the refresh controller can initiate the cycle. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals and one wait state for 16-bit peripherals. One wait state is inserted as a default for all DMA cycles. Any peripheral that cannot present read data or strobe in write data in this amount of time use IOCHRDY to extend these cycles.

This signal should not be held low for more than 2.5 us for normal operation. Any extension to more than 2.5 us does not guarantee proper DRAM memory contents because memory refresh is stopped while IOCHRDY is low.

4.2.7. MEMCS16# (16-Bit Memory Chip Select)

Input to CPU modules

Open collector output on any other module.

The MEMCS16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module is requesting a 16-bit memory cycle and the MEMCS16# line is high. If MEMCS16# is high, 16-bit CPU cycles are converted into two, 8-bit cycles on the bus automatically. If MEMCS16# is low, an access to peripherals is done 16-bit wide.

4.2.8. IOCS16# (16-Bit I/O Chip Select)

Input to CPU modules.

Open collector output on any other module.

The IOCS16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module is requesting a 16-bit I/O cycle and the IOCS16# line is high. If IOCS16# is high, 16-bit CPU cycles are converted into two, 8-bit cycles on the bus automatically. If IOCS16# is low, an access to peripherals is done 16-bit wide.

4.2.9. REF# (Memory Refresh)

Output to CPU modules.

Input on any other module.

REF# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us to prevent loss of DRAM data.

4.2.10. ZWS# (0 Wait States)

Input to CPU modules.

Output on any other module.

The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts four wait states for 8-bit transfers and one wait state for 16-bit transfers.

4.3 *Special Function Signal Group*

4.3.1. MASTER# (MASTER Bus Request)

Input to CPU modules.

Open collector output on any other module.

This signal is used with a DRQ line to gain control of the system bus. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which allows it to control the system address, data, and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost because of lack of refresh.

4.3.2. SYSCLK (System Clock)

Output from a CPU module.

Input on any other module.

SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with 40-60 % duty cycle. Different CPU modules may supply slower and higher frequencies. This signal is supplied at all times except when the CPU module is in sleep mode.

4.3.3. OSC (Oscillator Frequency)

Output from CPU modules.

Input to any other module.

CPU modules supply OSC. It has a nominal frequency of 14,31818 MHz and a duty cycle of 40-60 %. This signal is supplied at all times except when the CPU module is in sleep mode.

4.3.4. RSTDRV (Bus RESET)

Output from CPU modules.

Input to any other module.

This active high output is system reset generated from CPU modules to reset external devices.

4.3.5. DRQ <0, 2, 5, 7> (DMA Request)

Inputs to CPU modules.

Outputs from any other module.

The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DRQ<0..3> are used for transfers between 8-bit I/O adapters and system memory. DRQ<5..7> are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on CPU modules.

4.3.6. DACK# <0, 2, 5, 7> (DMA Acknowledge)

Outputs from CPU modules.

Inputs to any other module.

DMA acknowledge 0..3 and 5..7 are used to acknowledge DMA requests. They are low active.

4.3.7. TC (Terminal Count)

Output from CPU modules.

Input to all other modules.

The active high output TC indicates that one of the DMA channels has transferred all data.

4.3.8. IRQ <3..7, 9..12, 14,15> (Interrupt Requests)

Input to CPU modules.

Output on any other module.

These are the asynchronous interrupt request lines. IRQ0, 1, 2, 8 and 13 are not available as external interrupts because they are used internally on CPU modules. All IRQ signals are active high. The interrupt requests are prioritized, with IRQ9 through IRQ12 and IRQ14 through IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 through IRQ7 having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

4.4 Data Conversion and Swapping

4.4.1. Data Conversion

The 16-bit transfers by the main CPU via the PC/104 bus are converted into two, 8-bit transfers (low and high byte) when the control signals MEMCS16# or IOCS16# are not asserted. The higher byte-data (SD<15..8>) is directed to SD <7..0> with SA0 =H during write cycles and from SD <7..0> to SD <15..0 > with SA0 =H during read cycles. This operation is transparent to the software .

4.4.2. Data Swapping

Data are swapped between SD <15..8 > and SD <7..0 > on the main CPU for odd byte transfers (SA0 =H) with 8-bit devices on the PC/104 bus. Swapping occurs also during DMA cycles (SA0 =H) if the devices on the PC/104 bus is a 16-bit memory device and an 8-bit DMA channel is used for the transfer.

4.5 IDE Hard Disk Signals

4.5.1. IDECS0# (IDE Chip Select 0)

This is the Hard Disk Chip select corresponding to the eight control block addresses.

4.5.2. IDECS1# (IDE Chip Select 1)

This is the Hard Disk Chip select corresponding to the alternate status register.

4.5.3. DASP

Time-multiplexed, open collector output, which indicates that a drive is active, or that a slave drive is present. It is necessary for using IDE master/slave-mode on DIMM CPU modules with onboard IDE compatible Flash Filing System.

4.5.4. PDIAG

Output by the drive if it is jumped in the slave mode; input to the drive if it is jumped in the master mode. The signal indicates to a master that the slave has passed its internal Diagnostic command. It is necessary for using IDE master/slave-mode on DIMM CPU modules with onboard IDE compatible Flash Filing System.

4.6 *Serial Port Signals*

The following signals apply to the COM1 and COM on the DIM-PC module and COM3 and COM4 on the DIMM-I/O module.

4.6.1. DTR# (Data Terminal Ready)

Active low data terminal ready outputs for the serial port. The handshake output signal notifies modem that the UART is ready to establish data communication link.

4.6.2. RI# (Ring Indicator)

This active low input is for the serial port. The handshake signal notifies the UART that the telephone ring signal is detected by the modem.

4.6.3. TXD (Transmit Data)

Transmitter serial data output from serial port.

4.6.4. RXD (Receive Data)

Receiver serial data input.

4.6.5. CTS# (Clear To Send)

This active low input for serial ports . The handshake signal notifies the UART that the modem is ready to receive data.

4.6.6. RTS# (Request To Send)

This active low output for serial port. The handshake signal notifies the modem that the UART is ready to transmit data.

4.6.7. DCD# (Data Carrier Detect)

This active low input for serial port. The handshake signal notifies the UART that carrier signal is detected by the modem.

4.6.8. DSR# (Data Set Ready)

This active low input is for serial port. The handshake signal notifies the UART that the modem is ready to establish the communication link.

4.7 Floppy Disk Signals

4.7.1. FDHDSEL# (Head Select)

This active low output determines which disk drive head is active.

4.7.2. FDRDATA (Read Data)

This active low data read signal from the disk is connected here.

4.7.3. FDWRPRT (Write Protect)

This active low input senses from the disk drive that a disk is write-protected.

4.7.4. FDTRK0# (Track 0 Indicator)

This active low input senses from the disk drive that the head is positioned over the outermost track.

4.7.5. FDWGATE# (Write Gate)

This active low output enables the write circuitry of the disk drive.

4.7.6. FDWDATA# (Write Data)

This active low output is a write-precompensated serial data to be written onto the selected disk drive.

4.7.7. FDSTEP# (Head Step Signal)

This active low output produces a pulse at a software programmable rate to move the head during a seek operation.

4.7.8. FDDIR# (Head Step Direction)

This active low output determines the direction of the head movement.

4.7.9. FDMTR0# (Motor Enable Signal)

This active low output selects the motor of the disk drive.

4.7.10. FDDSKCHG# (Floppy Disk Change Signal)

This disk interface input indicates when the disk drive door has been opened.

4.7.11. FDDS0# (Floppy Drive Select Signal)

Active low output to select the disk drive.

4.7.12. FDCIDX# (Index Indicator)

This active low input senses from the disk drive that the head is positioned over the beginning of a track, as marked by the index hole.

4.8 *LPT Port Signals*

4.8.1. STB# (Strobe Signal)

This active low pulse strobes the printer data into the printer.

4.8.2. AFD# (Auto Feed Output)

This active low output causes the printer to automatically feed one line after each line is printed.

4.8.3. PD <0..7> (Printer Data Bus)

This bi-directional parallel data bus transfers information between CPU and peripherals.

4.8.4. ERR# (Error)

This active low signal indicates an error situation at the printer.

4.8.5. INIT# (Initiate Output)

This active low signal initiates the printer when low.

4.8.6. SLIN# (Printer Select Input)

This active low signal selects the printer.

4.8.7. ACK# (Acknowledge)

This active low output from the printer indicates it has received the data and is ready to receive new data.

4.8.8. BUSY (Busy)

This signal indicates the printer is busy and not ready to receive new data.

4.8.9. PE (Paper End)

This signal indicates that the printer is out of paper.

4.8.10. SLCT (Printer Select Status)

This active high output from the printer indicates that it has power on.

4.9 *Additional DIMM-PC Signals*

4.9.1. KBDAT (Keyboard Data)

This is the bi-directional keyboard data signal driven by an open collector output.

4.9.2. KBCLK (Keyboard Clock)

This is the keyboard clock signal driven by an open collector output.

4.9.3. SPKR (Speaker)

The speaker output signal is connected to a speaker between output and VCC.

4.9.4. GPCS0# (General Purpose Chip Select)

This general-purpose chip select output is used to select external peripherals.

4.9.5. PGOOD (Power Good)

High active input for the DIMM CPU indicates that power from the power supply is ready. It also can be used as low active reset input signal.

4.9.6. SMISW (SMI Interrupt Switch)

This input generates the CPU's SMI interrupt.

4.9.7. I2CLK (I2C Bus Clock)

This is a I2C-Bus Clk output signal to control external I2C-bus slave devices.

4.9.8. I2DAT (I2C Bus Data)

This is a I2C-Bus Data to control external I2C-Bus slave devices.

4.9.9. LNLED (Ethernet)

Active-low output indicating transmission or reception of frames or detection of a collision. It may be connected to external LED.

4.9.10. LKLED (Ethernet)

Active-low output indicates valid 10BASE-T link pulses. It may be connected to an external LED.

4.9.11. USB1- (USB Channel 1 Data)

This is the negative line of the differential data signal for the USB Channel 1

4.9.12. USB1+ (USB Channel 1 Data)

This is the positive line of the differential data signal for the USB Channel 1

4.10 *DIMM I/O Signals - Ethernet*

4.10.1. TXD+, TXD-

Differential output pair drives 10 Mb/s Manchester-encoded data to the 10BASE-T transmit lines.

4.10.2. RXD+, RXD-

Differential input pair receives 10 MB/s Manchester encoded data from the 10BASE-T receive lines.

4.10.3. LNLED

Active-low output indicating transmission or reception of frames or detection of a collision. May be connected to external LED.

4.10.4. LKLED

Active-low output indicating valid 10BASE-T link pulses. May be connected to external LED.

4.11 *DIMM I/O Signals - LCD Interface*

4.11.1. LFS

LCD Frame Start: This output provides a pulse to start a new frame on flat panels.

4.11.2. LLCLK

LCD Line Clock. This output drives the LCD panel-line clock. This signal also is designated as LP or CP1 by some panel manufacturers.

4.11.3. VDCLK

Flat Panel Video Clock. This signal drives the flat panel shift clock that is designated as CP2 by some panel manufacturers.

4.11.4. FPVEE

Flat Panel VEE enable. This output is part of the panel power sequencing.

4.11.5. VPANEL

Switched VDD is part of the panel power sequencing. Connects to VCC or VDD on most panels. This pin is a switch output. The desired output voltage must be supplied at Pin 37 (VDD_SRC).

4.11.6. PO-P15, P18-P23

Panel Data Signals. The Panel Data bus transports parallel signals that are used for SSTN, DSTN, and up to 18-bit TFT flat panels in monochrome and color mode. For a specific signal mapping, please refer to the DIMM-VGA2 manual.

4.11.7. BLANK#

Display Enable. For those flat panels that require an external display enable, this pin provides a data enable.

4.11.8. FPVDD

Flat Panel VDD enable. This output is part of the panel power sequencing. Normally, this signal is only used internally.

4.11.9. FPBACK

Flat Panel Backlight enable. This output is part of the panel power sequencing. It connects to the panel's backlight enable. Do not use this signal as supply voltage for the backlight converter!

4.11.10. MAD 12...15

Panel Sense: Inputs for panel type selection

4.12 *DIMM I/O Signals - CRT Interface*

4.12.1. HSYNC

Horizontal Sync: This output supplies the horizontal synchronization pulse to the monitor. It is normally not needed for flat panels.

4.12.2. VSYNC

Vertical Sync: This output supplies the vertical synchronization pulse to the monitor. It is normally not needed for flat panels.

4.12.3. REG, GREEN, BLUE

CRT analog video outputs.

5. BUS TIMING SPECIFICATION

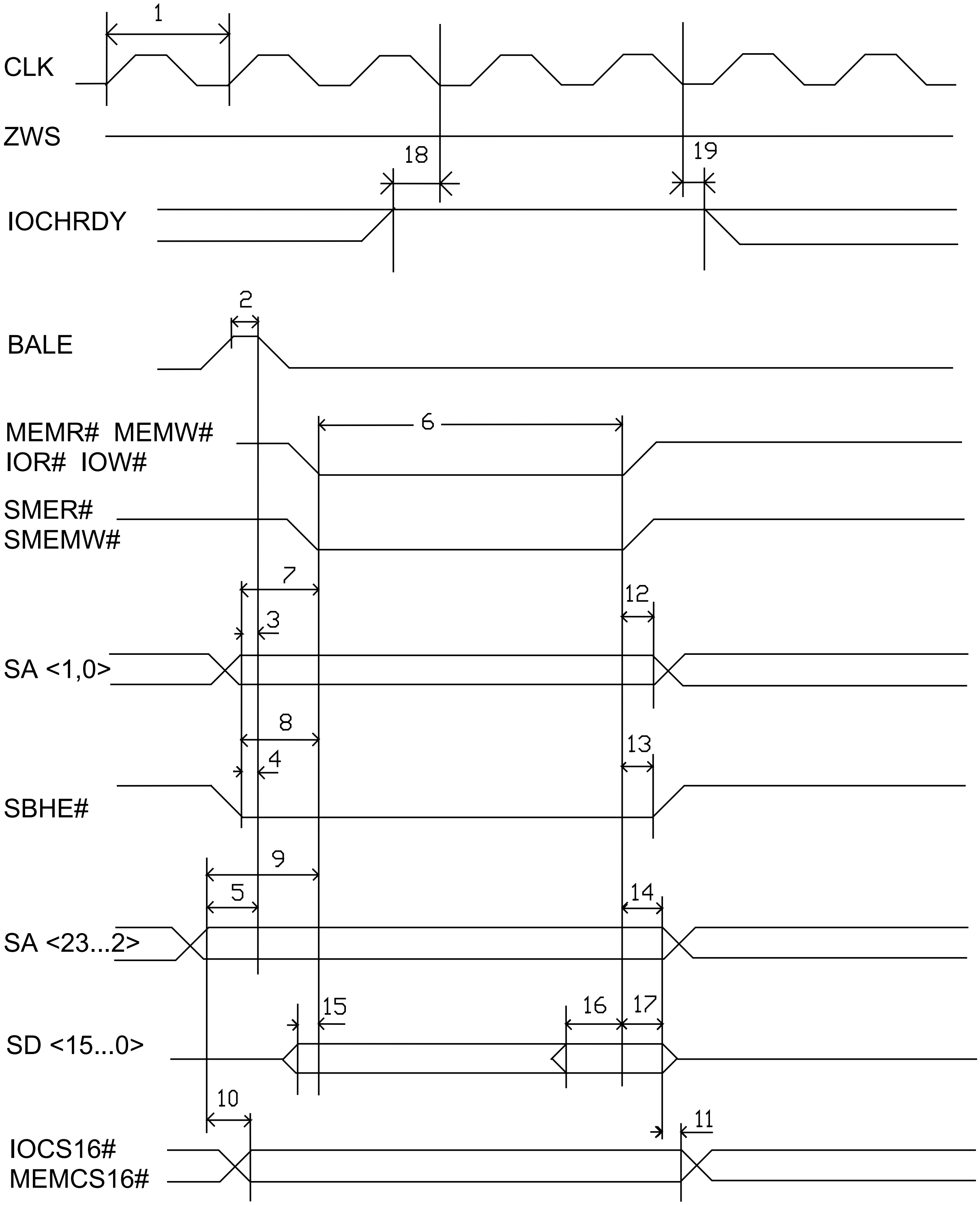
No.	Description	Min	Type	Max	Note
1	Clock period (T_{clk})	125			
2	BALE high width		54		
3	SA<1..0> setup to BALE low			8	
4	SBHE# setup to BALE low		20		
5	SA<23..2> setup to BALE low		130		
6a	Command width 16 bit cycles (zero wait states)		125		2)
6b	Command with 8 bit cycles (with 2 wait states)		325		3)
7	SA<1..0> setup to command zero cmd delay	8			1)
8	SBHE# setup to command zero cmd delay		20		1)
9	SA<23..2> setup to command zero cmd delay	130			1)
10	MEMCS16# , IOCS16# delay from SA<23..2>			80	
11	MEMCS16# , IOCS16# hold after SA<23..2	0			
12a	SA<1..0> hold after command	23			
12b	SA<1..0> hold after SMEMR# or SMEMW#		18		
13a	SBHE# hold after command	23			
13b	SBHE# hold after SMEMR# or SMEMW#	18			
14a	SA<23..2> hold after command	30			
14b	SA<23..2> hold after SMEMR# or SMEMW#	25			
15	Write Data setup to command active		6		
16	Read Data setup to command inactive	65			1)
17a	Write Data hold after command	45			
17b	Read Data hold after command	0			
18	IOCHRDY setup to CLK	34			
19	IOCHRDY hold after CLK	2			
20	ZWS# setup to CLK	20			
21	ZWS# hold after CLK	0			

Notes:
1.) Command delay programmable between 0 and 3 CLK/2 cycles separately for 16-bit memory, 8-bit memory, and I/O cycles.

2.) Command width depends on the number of wait states (programmable from 0 to 3 CLK cycles) and command delay (Note 1).

3.) Command width depends on the number of wait states (programmable from 2 to 5 CLK cycles) and command delay (Note 1).

CPU Bus Cycle Timing



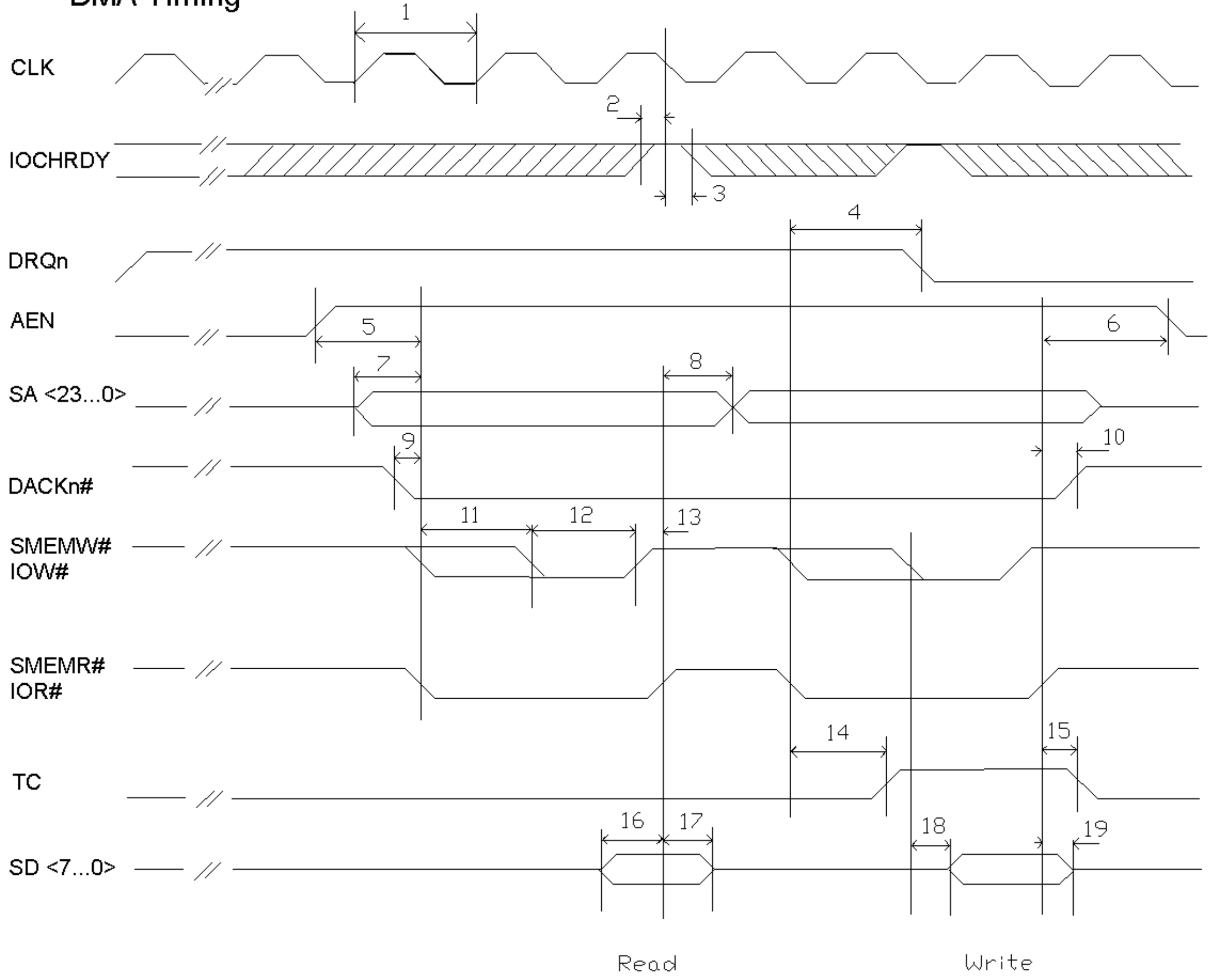
5.1 DMA Timing Specification

This section specifies the timing for Direct Memory Access cycles (all times in ns).

No.	Description	MIN	TYP	MAX	Note
1	Clock period (T_{clk})	125			
2	IOCHRDY setup to CLK	35			
3	IOCHRDY hold from CLK	20			
4	DRQ inactive delay from command			55	
5	AEN setup to command	80			
6	AEN hold from command	10			
7	SA<23..0> setup to command	50			
8	SA<23..0> hold from command	50			
9	DACK setup to command	0			
10	DACK hold from command		0		
11	Extended Write delay	122		128	
12	Write command width (Extended Write , 0 Waitstates)	80			1)
13	Read inactive delay from Write	20			
14	T/C delay from command			165	
15	T/C hold from command	0			
16	Read data setup	110			
17	Read data hold	0			
18	Write data delay after command			80	2)
19	Write data hold	15			

Notes:
1.) With programmable wait states from 1 to 4 CLK cycles.
2.) This time cannot be extended by insertion of wait states.

DMA Timing



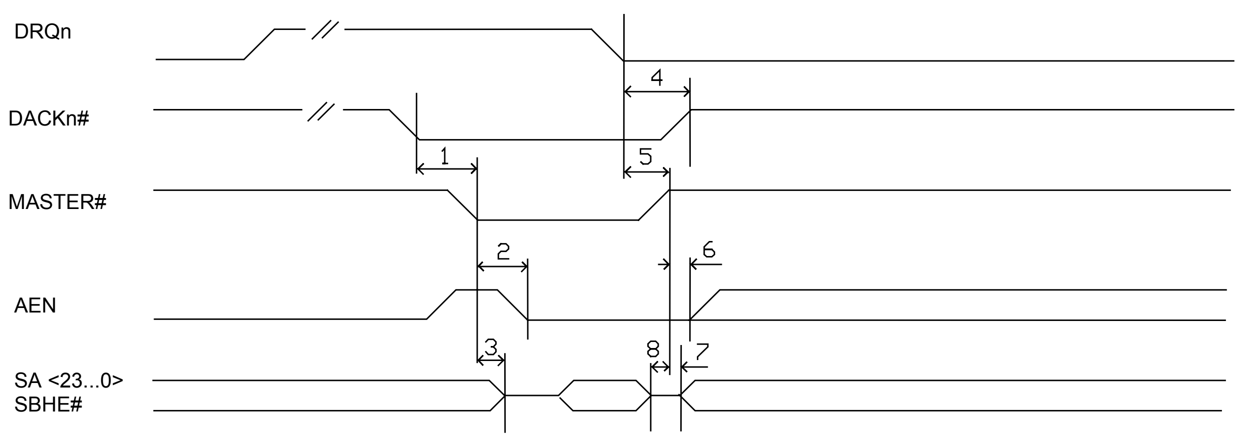
CLK
IOCHRDY
DRQn
AEN
SA <23...0>
DACKn#
SMEMW#
IOW#
SMEMR#
IOR#
TC
SD <7...0>
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
Read
Write

5.2 *Bus Master Exchange Operation*

This section specifies the timing for exchange of bus ownership between the CPU and a secondary bus master (all times in ns):

No.	Description	MIN	MAX
1	MASTER# delay after DACKn#	0	
2	AEN inactive after MASTER# active		45
3	CPU tristates bus signals		45
4	DACKn# inactive from DRQn inactive	0	
5	MASTER# delay from DRQn inactive		100
6	AEN delay after MASTER# inactive	0	45
7	CPU drives bus signals	0	
8	Secondary Master tristates bus signals	0	

BUS Master Exchange Operation

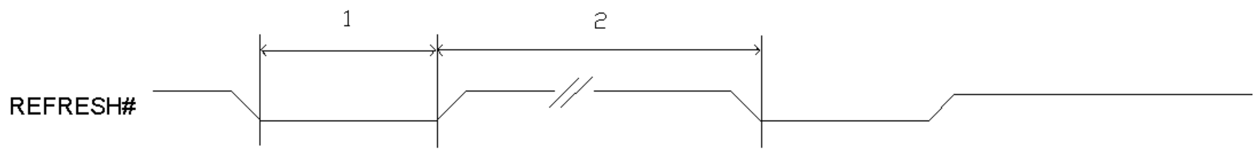


5.3 REFRESH# Signal Timing

This section specifies the timing of the REFRESH# signal.

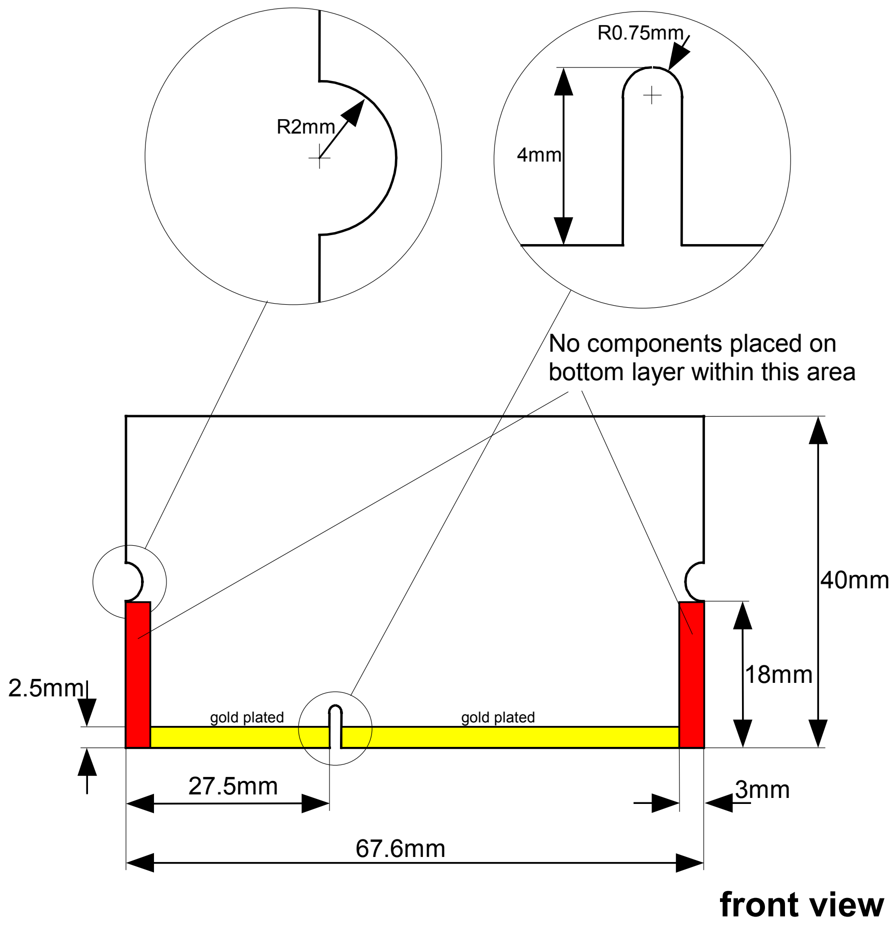
No.	Description	MIN
1	REFRESH# pulse width	750ns
2	REFRESH# inactive time	15,6µS

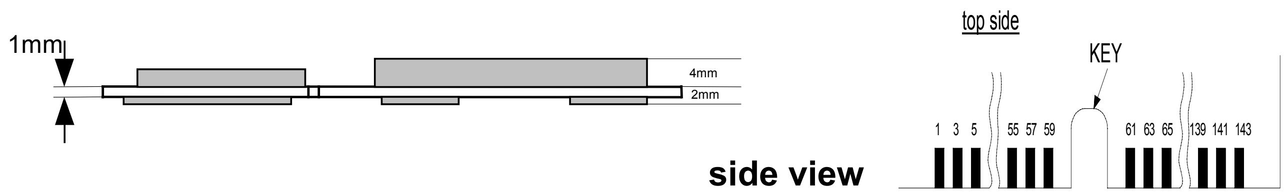
REFRESH# Signal Timing



6. MECHANICAL DIMENSIONS

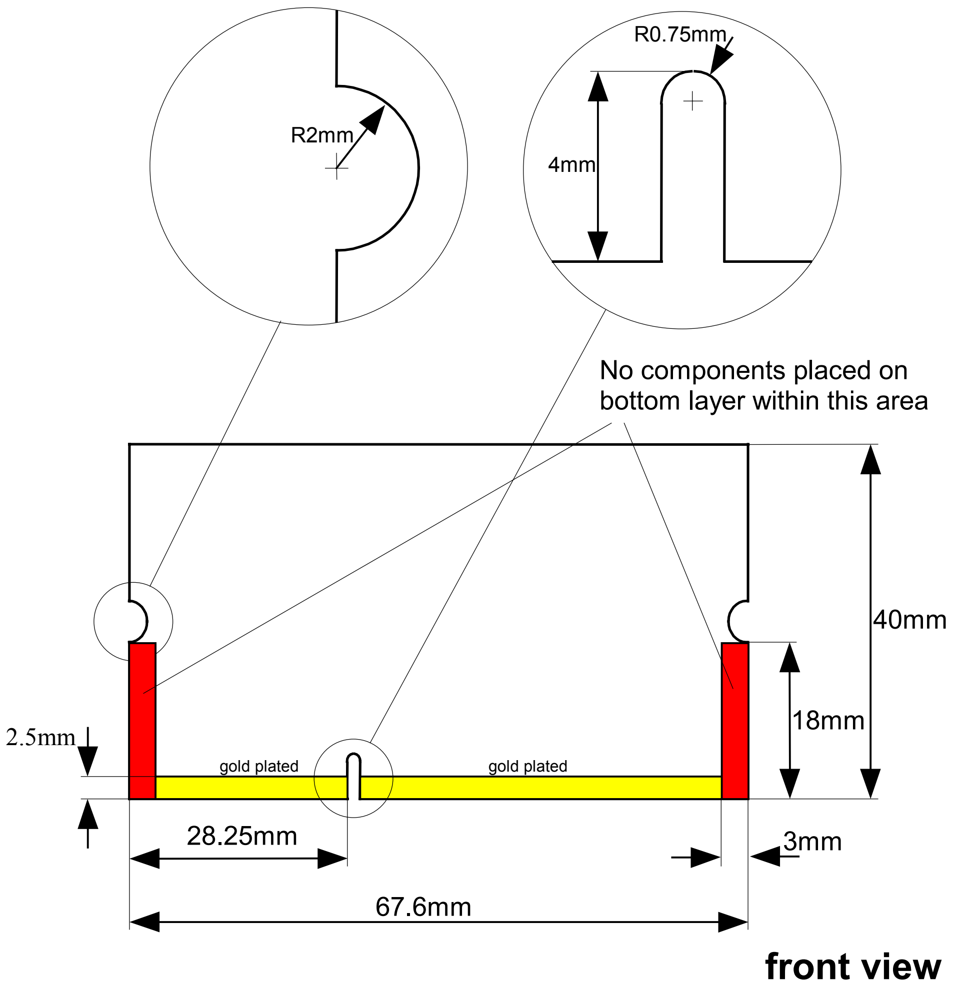
6.1 CPU Modules

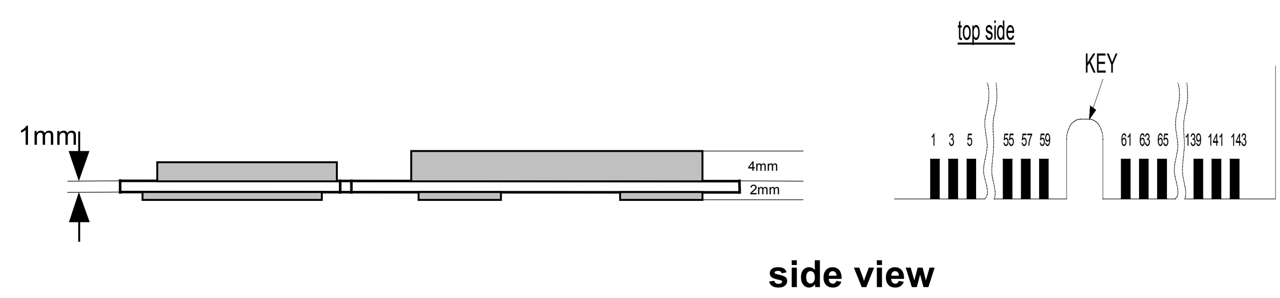




The DIMM-CPU Module has a maximum thickness of 6 mm, while the top components are up to 4 mm high and the bottom components are up to 1 mm high.

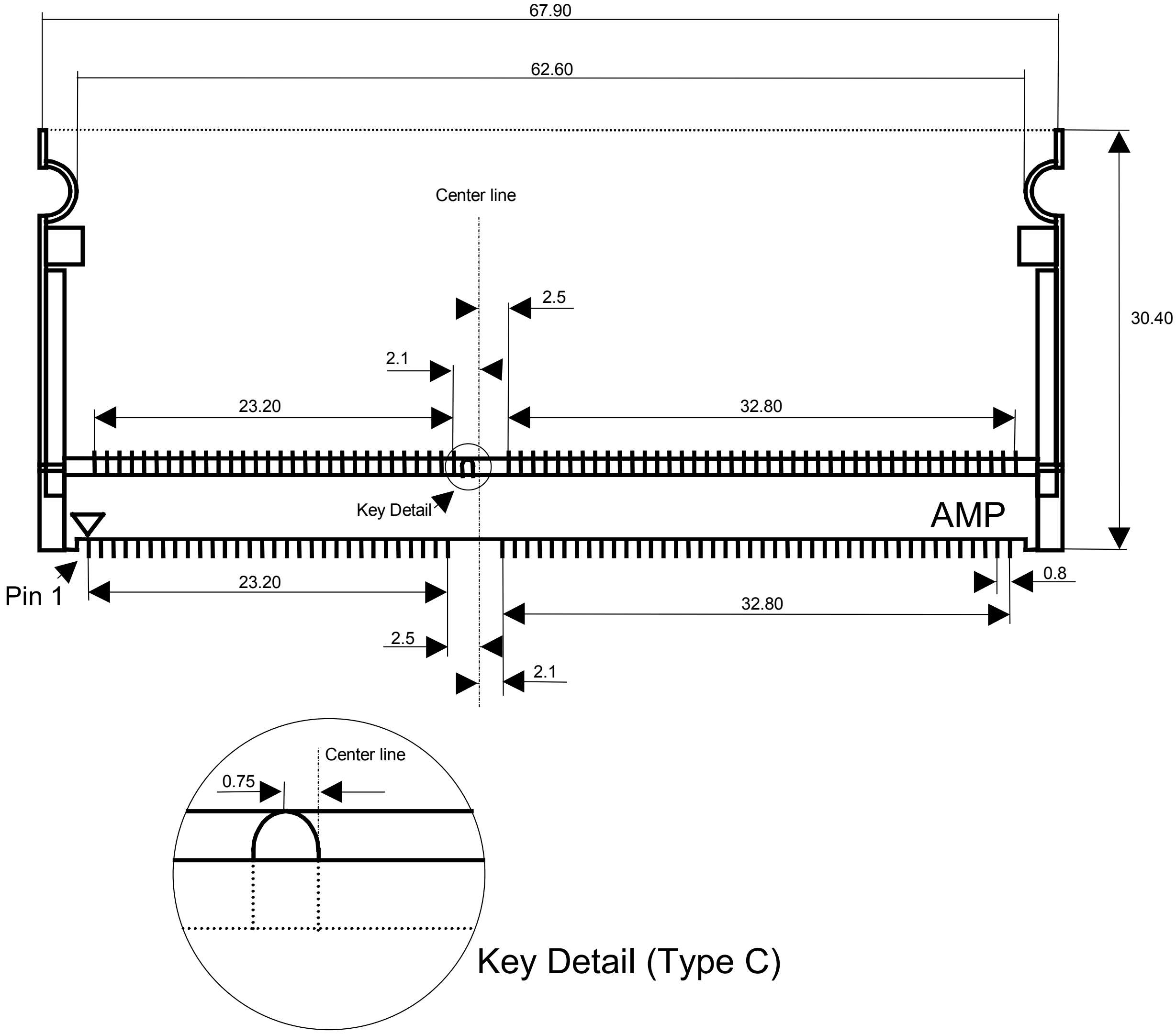
6.2 I/O Modules

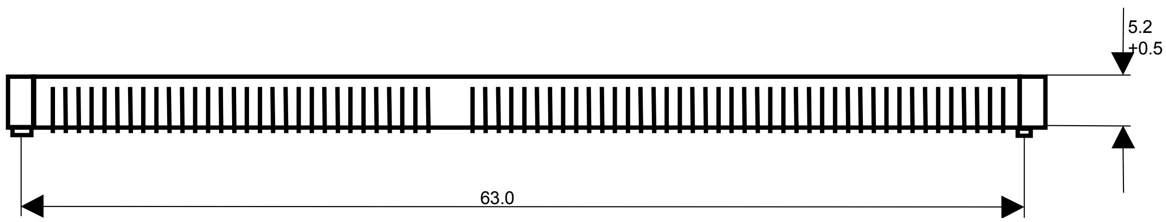




6.3 *DIMM Connector Dimensions*

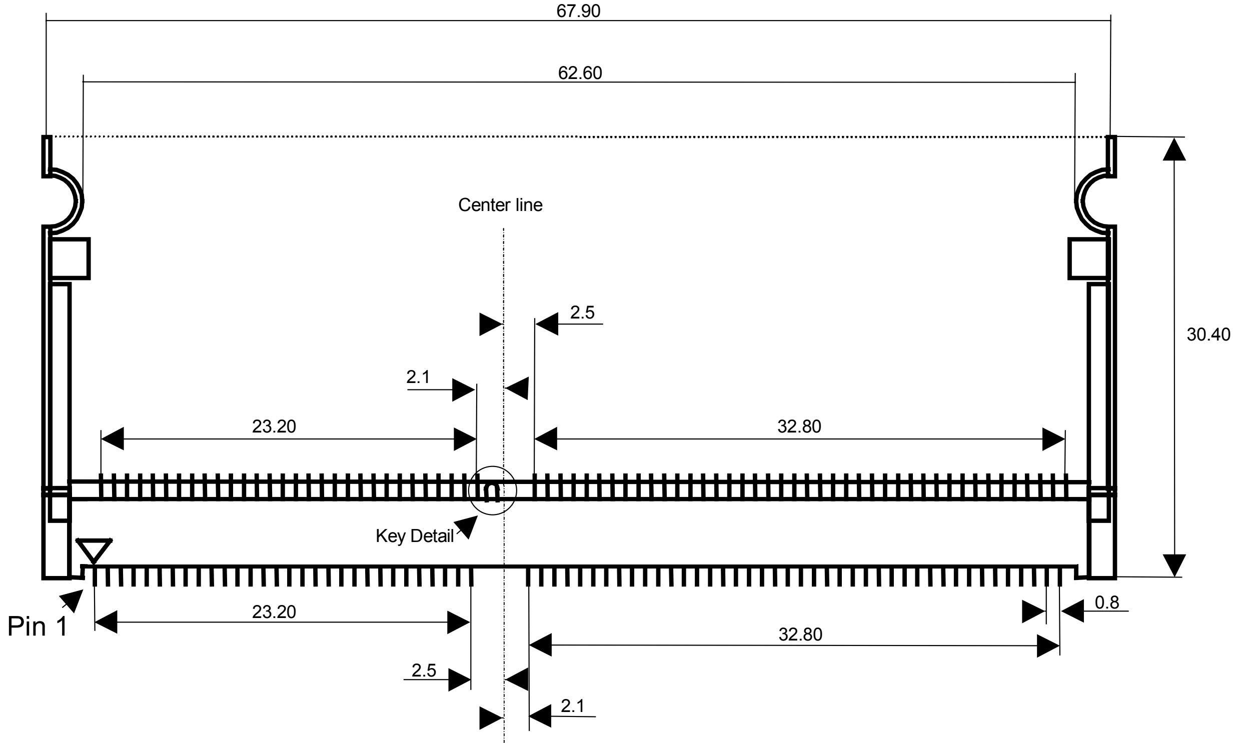
6.3.1. CPU Modules

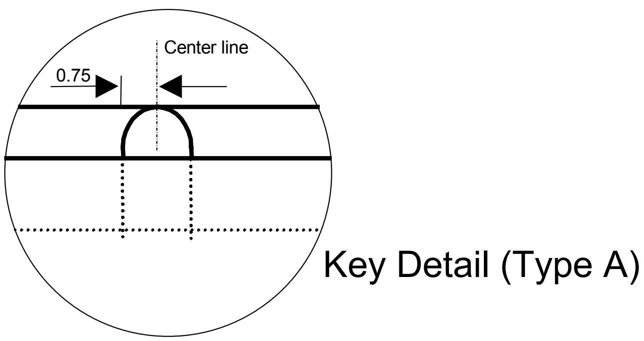


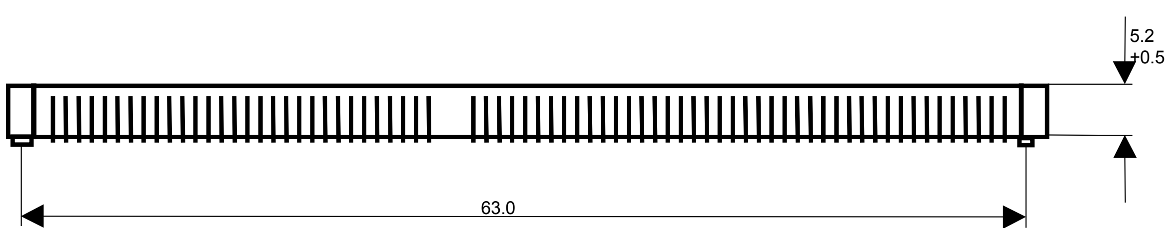


For further information please refer to Kontron specification document X00762.

6.3.2. I/O Modules







For further information please refer to Kontron specification document X00787.

7. ELECTRICAL CHARACTERISTICS

7.1 Power Supply Pins

	DIMM	Current Max
GND	6	
VCC	3	1.5 A

7.2 Electrical Specifications

7.2.1. Supply Voltage

- 5V DC +/- 5%

7.2.2. Supply Voltage Ripple

- 100 mV peak to peak 0 – 20 MHz

7.3 Environmental Specifications

7.3.1. Temperature

- Operating 0 to +60 C (*) (with appropriate airflow)
- Non operating: -10 to +85 °C

7.3.2. Humidity

- Operating: 10% to 90% (non-condensing)
- Non operating: 5% to 95% (non-condensing)

Notes:
(*)The maximum operating temperature is the maximum measurable temperature on any spot on the modules surface. It is the user's responsibility to maintain this temperature within the above specification.

8. PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand DIMM-PC architecture.

8.1 *DIMM-PC Specification*

- DIMM-PC Specification, www.kontron.com

8.2 *PC/104-Bus*

- PC/104 Specification Version 2.3 June 1996
- PC/104 Consortium; www.pc104.org
- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)

8.3 *ISA-Bus, Standard PS/2 - Connectors*

- ISA System Architecture, Addison-Wesley Publishing Company
- Edward Solari, AT BUS Design IEEE P996 Compatible, Annabooks San Diego CA. ISBN 0-929392-08-6 www.annabooks.com
- PC Handbook, Sixth Edition, John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1 www.annabooks.com
- AT IBM Technical Reference Vol 1&2, 1985
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)

8.4 RS232C, RS485

- EIA-232-E Interface between data terminal equipment and date circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)
- EIA-422-A Electrical characteristics of balanced voltage digital interface circuits
- EIA-423-A Electrical characteristics of unbalanced voltage digital interface circuits
- EIA-485 Standard for electrical characteristics of generators and receivers for use in balanced digital multipoint systems
- EIA-449 General purpose 37-position and 9-position interface for data terminal equipment and data circuit-terminating equipment.
- EIA-530 High speed 25-position interface for data terminal equipment and data circuit-terminating equipment
- EIA/TIA-562 Electrical characteristics for an unbalanced digital interface
- National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering „232“, „422“ or „485“ as search criteria to get a current list of related application notes.

8.5 PC Hardware

- PC Hardware, Messmer Hans-Peter, Addison-Wesley-Longman GmbH, 1998, ISBN 3-8273-1302-3 (German)

8.6 Miscellaneous

- AMP Catalog ”IC Sockets” 82172 rev 9-96, page 70
- BERG SIMM/DIMM con. 950524-0001 10/96, page 7-34

9. DOCUMENT-REVISION HISTORY

Filename	Date	Edited by	Alteration to Preceding Revision
DIMMD110.DOC	11.03.97	H. Muehlbauer	Created manual.
DIMMD111.DOC	04.04.97	H. Muehlbauer	Added ISA bus timing.
DIMMD112.DOC	11.04.97	H. Muehlbauer	Added connector types.
DIMMD113.DOC	20.05.97	H. Muehlbauer	Added I2C Bus signal to DIMM connector.
DIMMD114.DOC	07.10.97	M. Hofmeister	Changed connector order numbers.
DIMMD115.DOC	20.10.97	M. Hofmeister	Added pinout of DIMM I/O module.
DIMMD116.DOC	20.11.97	M. Hofmeister	Added signal description, specification of DIMM-I/O.
DIMMD117.DOC	18.02.98	M. Hofmeister	Changed pinout of DIMM-I/O.
DIMMD118.DOC	27.03.98	M. Hofmeister	Changed CAN-signals to INTERBUS signals
DIMMD119.DOC	26.05.98	F. Krauss	Changed pinout of DIMM-I/O.
DIMMD11A.DOC	04-01.00	M. Hofmeister	Added small drawing in mechanical characteristics to identify location of Pin 1.
DIMMD11B.DOC	07.01.00	J. Baumgartner	Added Ethernet control signals to DIMM-CPU pinout.
DIMMD11C.DOC	19.10.00	R. Barth	Deleted manufacturer of sockets in Chapter 5; added mech. schematics with dimensions; added reference to JUMP*tec*® specs of sockets.
DIMMD11D.DOC	03.04.01	J. Baumgartner	Added USB signals to DIMM-CPU, added restricted areas to mechanical drawings.
DIMMD120.DOC	12.02.02	J. Baumgartner	Changed pinout of DIMM-I/O module for DIO4; corrected ISA signal names
DIMMD121.DOC	02.09.03	D. Gunter J. Lowell	Updated manual throughout.