

» Kontron User's Guide «



nanoETXexpress-SP

Document Revision 141

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1 User Information

1.1 About This Document

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For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

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- » Microsoft is a registered trademark of Microsoft Corp.
- » Intel is a registered trademark of Intel Corp.
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1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at <http://www.kontron.com/support> for the latest product documentation, utilities, drivers and support contacts. Consult our customer section <http://emdcustomersection.kontron.com> for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 Product Description

This credit card sized module is compatible to COM Express™ pin-out Type 1. On 55 mm x 84 mm footprint nanoETXexpress-SP is a perfect fit for the next generation of low power, ultra-mobile applications that require energy saving x86 processor performance, high-end graphics, PCI Express and Serial ATA combined with longer battery life. These include handheld devices for medical or multi-media applications, small mobile data systems and a host of new applications that have not previously been possible due to size or power consumption limitations. This new COM form factor is 100 percent compatible with the COM.0 Type 1 with respect to connector location and pin definition. The Kontron nanoETXexpress-SP COM is based on the highly-efficient Intel® Atom™ Z5XX processor series and Intel® System Controller Hub single chip that combines the memory controller, graphic engine and I/O in a single, space saving chipset design. The nanoETXexpress-SP COM offers an unprecedented power consumption / performance ratio for x86-based ultra-mobile designs. The nanoETXexpress-SP with Flash and memory on-board supports 1 PCI Express x1 Port (opt. 2 x1 if no onboard LAN), Serial ATA, LVDS, optional SDVO and High Definition Audio. 10/100/1000 Gigabit Ethernet is designed onboard for high connectivity and 8x USB provides fast and sufficient interfaces for external peripherals.

2.2 Naming clarification

COM Express™ defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component. Interfaces will provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA and PCI Express and Serial ATA.

- » ETXexpress® modules are Kontron's COM Express™ modules in basic form factor (125mm x 95mm)
- » microETXexpress® modules are Kontron's COM Express™ modules in compact form factor (95mm x 95mm)
- » nanoETXexpress® modules are Kontron's COM Express™ modules in the future ultra form factor (55mm x 84mm)

2.3 Understanding COM Express™ Functionality

All Kontron microETXexpress® and ETXexpress® modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D. On nanoETXexpress® modules only the primary connector Row A and Row B is used.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

- » Ethernet
- » Serial ATA (SATA)
- » USB 2.0
- » LVDS/VGA and dual display video
- » High Definition Audio (Azalia)
- » LPC (low pin count) Bus
- » PCIexpress

2.4 COM Express™ Documentation

This product manual serves as one of three principal references for a COM Express™ design. It documents the specifications and features of nanoETXexpress-SP. The other two references, which are available from your Kontron Support or from PICMG®, include:

- » The COM Express Specification defines the COM Express™ module form factor, pinout, and signals. This document is available from the PICMG website by filling out the order form.
- » The COM Express™ Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express™ modules.



Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express™ Benefits

Computer on modules express (COM Express™) modules are very compact, highly integrated computers. All (nano/micro)ETXexpress® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each (nano/micro)ETXexpress® module is based on connector type 1 or 2 of the COM Express™ specification. This standardization allows designers to create a single-system baseboard that can accept present and future (nano/micro)ETXexpress® modules.

(nano/micro)ETXexpress® modules include common personal computer (PC) peripheral functions such as:

- » Graphics
- » USB ports
- » Ethernet
- » Sound
- » SATA

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress®, microETXexpress® and nanoETXexpress modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COM Express™ solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express™ baseboard can work with several successive generations of COM Express® modules.

A COM Express™ baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Available Modules of nanoETXexpress-SP

nanoETXexpress-SP is available in different variants to cover the demand of different performance, price and power. The following table shows the different combinations of nanoETXexpress-SP

Product Number	Intel® ATOM™ CPU	Onboard DDR2 SDRAM	Onboard Flash Drive	Lan Controller
34001-5151-11-0	1,1GHz Z510	512MB	512MB	no
34001-5151-11-1	1,1GHz Z510	512MB	512MB	yes
34001-5151-11-1EXT	1,1GHz Z510	512MB	512MB	yes
34001-5120-11-1	1,1GHz Z510	512MB	2GB	yes
34001-1020-11-1	1,1GHz Z510	1GB	2GB	yes
34001-5120-16-1	1,6GHz Z530	512MB	2GB	yes
34001-1040-16-1	1,6GHz Z530	1GB	4GB	yes

3.2 Functional Specification

Processor: Intel® ATOM™

Processor	Number of Cores	Core	Processor Base Frequency	L2 Cache	Bus Speed	VT-x	HT	Intel® 64	EIST	Max TDP
Z510	1	45nm	1.1 GHz	512KB	400 MHz	No	No	No	Yes	2W
Z530	1	45nm	1.6 GHz	512KB	533 MHz	Yes	Yes	No	Yes	2,2W

Chipset: SCH US15W

Speed:	400/533 MHz
RAM:	memory down up to 2GB Single Channel
USB:	2 x USB 2.0 (COM #4,#5) 5 x USB 1.1/2.0
USB Client:	1 x USB Client (COM #7)
Audio:	HD Audio
PCI Express:	1 PCIe X1 2 PCIe X1 without LAN
Max TDP:	2.3W

Integrated graphics: Intel® GMA 500

max graphic memory (GMA driver):	Intel® GMA 500
max graphic memory (IEGD):	352MB
Graphics Core Render Clock:	200MHz
Memory Bandwidth (GB/s):	4.2
Pixel Pipelines:	4
DirectX / OpenGL:	9.0c / 2.0
Shader Model:	3.0
Hardware acceleration:	H.264,MPEG2/4,VC1,WMV9

Display Interfaces

CRT:	VGA is not supported by the US15W System Controller Hub
Flat Panel:	Single Channel LVDS 18/24 Bit, resolution up to 1366 x 768 (WXGA), no dithering.
Digital Display:	Optional Serial DVO (SDVO) with resolution up to FullHD 1920 x 1080 is supported via 30pin onboard flat foil connector or project based on COM Express connector

Storage

Flash Disk:	Onboard SSD Flash drive up to 4GB (primary master)
SATA:	1xSerial ATA supporting 1.5Gbit/s (PATA2SATA Bridge, primary slave)

Onboard devices:

Ethernetcontroller:	Intel® 82574L (Hartwell) offers 10/100/1000 Mbit
Ethernetfeatures:	WakeOnLan, PXE Lanboot, Time Sync Protocol Indicator, Jumbo Frames
TPM:	Optional Trusted Platform Module 1.2
Watchdog:	Integrated in onboard CPLD

Additional Interfaces:

LPC:	Yes
SMBus:	Yes
I2C:	Fast I2C (from US15W SCH)
GPIO:	8 GPIO, 4 GPI and 4 GPO via JIDA32 interface IO Port 0
SDIO:	1 x SDIO port (SD 1.1) shared with GPIO signals; SDIO boot supported with BIOS NOW1R113 or newer

Kontron Features

I2C support:	Fast I2C
MARS support:	Extended
JIDA / EAPI support:	JIDA 16/32
K-Station:	YES
JILI support:	Extended
Flash Backup:	R113
S5 Eco Mode:	-
Darkboot / Bootlogo support:	YES
Watchdog support:	YES

3.3 Onboard SSD

The nanoETXexpress-SP is equipped with an onboard commercial or industrial flash drive from 512MB up to 4 GB capacity. The onboard flash drive is connected as the primary master device to the US15W PATA interface through a standard ATA/IDE bus interface. Basic features of the nanoETXexpress-SP onboard Flash Drive:

- » up to PIO Mode 6
- » up to multi word DMA Mode 4
- » up to ultra DMA-4
- » Build in ECC (Error Correction Code)
- » Dynamic Wear Leveling
- » Expanded Data Protection

The nanoETXexpress-SP is equipped with different commercial and industrial SSD flash types. Find the details according to the module hardware revision below:

Series modules equipped with Intel® Atom™ Z510 CPU

	34001-5151-11-0	34001-5151-11-0	34001-5151-11-1	34001-5151-11-1
Module HW Revision	CE 1.0.x	CE 1.1.x and newer	CE 1.0.x	CE 1.1.x and newer
Flash Size	512MB commercial	512MB industrial	512MB commercial	512MB industrial
Flash Part No.	SST85LD0512T-120-5C	SST85LD0512-60-RI	SST85LD0512T-120-5C	SST85LD0512-60-RI
NAND Type	SLC NAND	SLC NAND	SLC NAND	SLC NAND
Host write Cycles	-	100M	-	100M
Flash Erase Cycles	100k	100k	100k	100k
Flash Temp Range [°C]	0 to 70	-40 to 85	0 to 70	-40 to 85
Sustained Read Speed	10 MB/s	17 MB/s	10 MB/s	17 MB/s
Sustained Write Speed	5 MB/s	5 MB/s	5 MB/s	5 MB/s

Series modules equipped with Intel® Atom™ Z530 CPU

	34001-5120-16-1	34001-5120-16-1	34001-1040-16-1	34001-1040-16-1
Module HW Revision	CE 1.0.x	CE 1.1.x and newer	CE 1.0.x (Samples)	CE 1.1.x and newer
Flash Size	2GB commercial	2GB industrial	4GB commercial	4GB industrial
Flash Part No.	SST85LD1002L-60-PC	SST85LD1002U-60RI	SST85LD1004M-60-PC	SST85LD1004T-60-RI
NAND Type	SLC NAND	SLC NAND	MLC NAND	SLC NAND
Host write Cycles	10M	100M	10M	100M
Flash Erase Cycles	10k	100k	10k	100k
Flash Temp Range [°C]	0 to 70	-40 to 85	0 to 70	-40 to 85
Sustained Read Speed	23 MB/s	30 MB/s	30 MB/s	20 MB/s
Sustained Write Speed	4 MB/s	20 MB/s	8 MB/s	20 MB/s

3.4 System Memory

The nanoETXexpress-SP provides up to 2GB of DDR2 SDRAM which is soldered on the module.

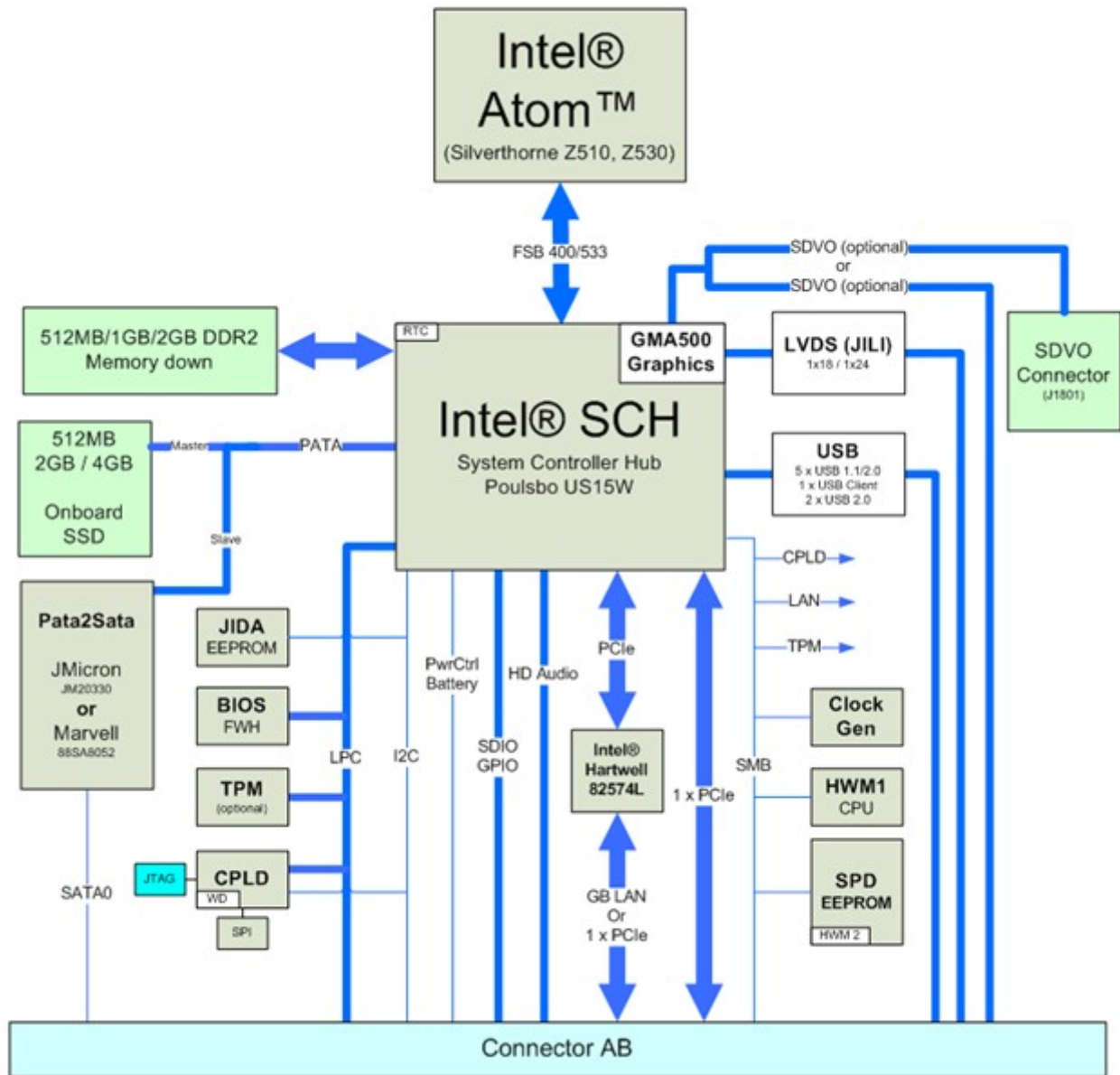
The total amount of memory available on the module is used for main memory and graphics memory. The Unified Memory Architecture (UMA) manages how the system shares memory between the graphics controller and the processor.

The maximum supported memory configuration is 8 x 2Gbit (2GB). Usually modules are equipped with 8 x 1Gbit (1GB) or 4 x 1Gbit (512MB mounted on bottom side of the PCB).



8 memory chips are only supported on hardware revision CE 4.x.x or newer. Former hardware revisions supports up to 4x2Gbit (1GB) system memory.

3.5 Block Diagram



3.6 Mechanical Specification

3.6.1 Module Dimension

» Listenpunkt 55mm x 84mm ($\pm 0.2\text{mm}$)

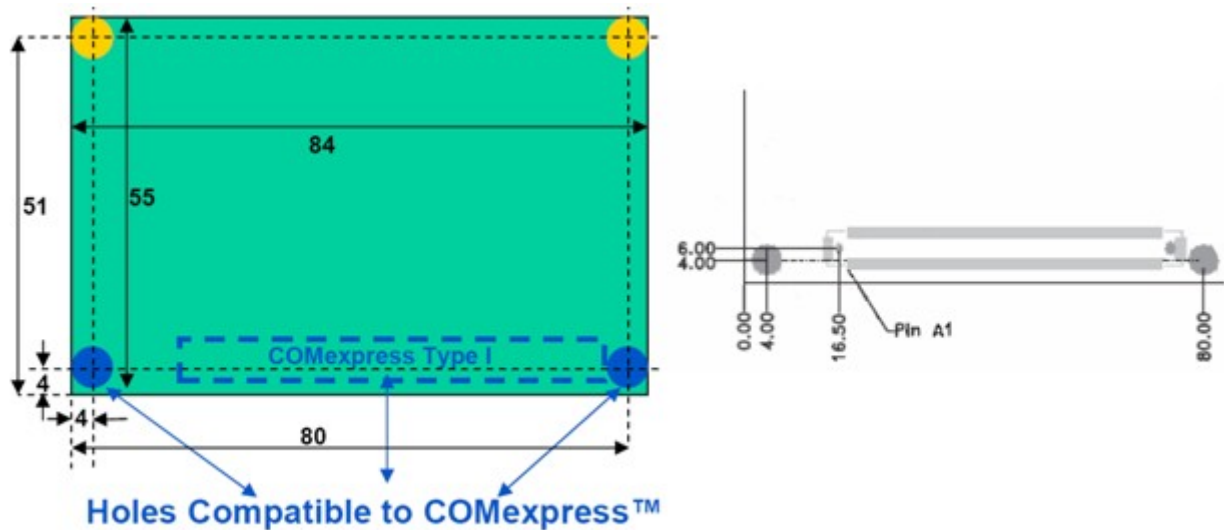
3.6.2 Height on Top

- » Maximum approx. 3.5mm (withouth printed circuit board)
- » Height is depending on (optional) CPU cooler / heat spreader

3.6.3 Height on Bottom

» Maximum appprox. 3.5mm (without printed circuit board)

3.6.4 Mechanical Drawing



All dimensions are shown in millimeters. Tolerances should be $\pm 0.25\text{mm}$ [$\pm 0.010''$], unless otherwise noted. The tolerances on the module connector locating peg holes (dimensions [16.50, 6.00]) should be $\pm 0.10\text{mm}$ [$\pm 0.004''$]. The 220 pin module connector shall be mounted on the backside of the PCB and is seen "through" the board in this view. The 4 mounting holes shown in the drawing should use 6mm diameter pads and should have 2.7mm plated holes, for use with 2.5mm hardware. The pads should be tied to the PCB ground plane.



A complete Solid Works eDrawing package is available at Kontron's [EMD Customer Section](#)

3.7 Electrical Specification

3.7.1 Supply Voltage

nominal Voltage:	12V +/- 5%
Wide Range input:	4.75 - 14V
5V_Stb:	5V DC +/- 5%



If a module is E1 rated and should be used in E1 temperature range the supply voltage must be 12V +/- 5%!

3.7.2 Power Supply Rise Time

- » The input voltages shall rise from $\leq 10\%$ of nominal to within the regulation ranges within 0.1ms to 20ms.
- » There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

3.7.3 Supply Voltage Ripple

- » Maximum 100 mV peak to peak 0 – 20 MHz

3.7.4 Power Consumption

The maximum Power Consumption of the different nanoETXexpress-SP modules is 4.9 - 6.2W (100% CPU load; 90°C CPU temperature). Further details with measurements and TDP values of the single variants can be found in our [customer section](#). Information there is available after registration.

3.8 Environmental Specification

3.8.1 Temperature

With Kontron Embedded Modules GmbH heatspreader plate assembly

Operating:

- » Ambient temperature: 0 to +60 °C
- » Maximum heatspreader-plate temperature: 0 to +60 °C

Non-operating: -30 to +85 °C



The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Without Kontron Embedded Modules GmbH heatspreader plate assembly

Operating:

- » Maximum operating temperature: 0 to +60 °C)

Non operating: -30 to +85 °C



The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

3.8.2 Humidity

- » Operating: 10% to 90% (non condensing)
- » Non operating: 5% to 95% (non condensing)

3.9 MTBF

The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The calculation method used is "Telcordia Method 1 Case 3" in a ground benign, controlled environment (GB,GC).

This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Other environmental stresses (extreme altitude, vibration, salt water exposure, etc) lower MTBF values.

System MTBF (hours): 209423 @ 40°C



Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

Connector The pin outs for nanoETXexpress-SP Interface Connectors X1A and X1B are documented for convenient reference. Please see the COM Express™ Specification and COM Express™ Design Guide for detailed, design-level information.

3.10 Pinout List

3.10.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection



To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

3.10.2 Connector X1A Row A

Pin	Signal	Description	Type	Termination (CE 4.x.x)	Comment
A1	GND_1	Power Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data-	DP-I	-	-
A3	GBE0_MDI3+	Ethernet Receive Data+	DP-I	-	-
A4	GBE0_LINK100#	Ethernet Speed LED 100Mbps	0-3.3	-	-
A5	GBE0_LINK1000#	Ethernet Speed LED 1000Mbps	0-3.3	-	-
A6	GBE0_MDI2-	Ethernet Receive Data-	DP-I	-	-
A7	GBE0_MDI2+	Ethernet Receive Data+	DP-I	-	-
A8	GBE0_LINK#	LAN Link LED	OD	-	-
A9	GBE0_MDI1-	Ethernet Receive Data-	DP-I	-	-
A10	GBE0_MDI1+	Ethernet Receive Data+	DP-I	-	-
A11	GND_2	Power Ground	PWR	-	-
A12	GBE0_MDIO-	Ethernet Transmit Data-	DP-0	-	-
A13	GBE0_MDIO+	Ethernet Transmit Data+	DP-0	-	-
A14	GBE0_CTREF	LAN Reference Voltage	0-1.8	-	-
A15	SUS_S3#	Indicates Suspend to RAM state	0-3.3	-	CPLD I/O
A16	SATA0_TX+	SATA 0 Transmit Data+	DP-0	-	-
A17	SATA0_TX-	SATA 0 Transmit Data-	DP-0	-	-
A18	SUS_S4#	Indicates Suspend to Disk state	0-3.3	-	CPLD I/O
A19	SATA0_RX+	SATA 0 Receive Data+	DP-I	-	-
A20	SATA0_RX-	SATA 0 Receive Data-	DP-I	-	-
A21	GND_3	Power Ground	PWR	-	-
A22	SATA2_TX+	Not Connected	nc	-	not supported
A23	SATA2_TX-	Not Connected	nc	-	not supported
A24	SUS_S5#	Indicates Soft Off state; same function as SUS_S4#	0-3.3	-	CPLD I/O
A25	SATA2_RX+	Not Connected	nc	-	-
A26	SATA2_RX-	Not Connected	nc	-	-
A27	BATLOW#	Indicates low external battery	I-3.3	PU 5k-25k in CPLD	CPLD I/O
A28	ATA_ACT#	SATA Activity Indicator	0-3.3	PU 10k 3.3V	-
A29	AC_SYNC	HD Audio Sync	0-3.3	PD 22k in US15W	-
A30	AC_RST#	HD Audio Reset	0-3.3	PD 22k in US15W	-
A31	GND_4	Power Ground	PWR	-	-
A32	AC_BITCLK	HD Audio Clock	0-3.3	PD 22k in US15W	24MHz
A33	AC_SDOUT	HD Audio Data	0-3.3	PD 22k in US15W	-
A34	BIOS_DISABLE#	Disable Module BIOS. Enables boot from a BIOS on Baseboard	I-3.3	PU 10k 3.3V	For external LPC FWH
A35	THRMTRIP#	CPU thermal shutdown indicator	0-3.3	PU 2k 3.3V	not supported on CE 1.x.x
A36	USB6-	USB Data- Port #6	DP-I/0	PD 15k in US15W	-
A37	USB6+	USB Data+ Port #6	DP-I/0	PD 15k in US15W	-

A38	USB_6_7_OC#	USB Over current Pair 6 / 7	I-3.3	PU 10k 3.3V	-
A39	USB4-	USB Data- Port #4	DP-I/O	PD 15k in US15W	-
A40	USB4+	USB Data+ Port #4	DP-I/O	PD 15k in US15W	-
A41	GND_5	Power Ground	PWR	-	-
A42	USB2-	USB Data- Port #2	DP-I/O	PD 15k in US15W	-
A43	USB2+	USB Data+ Port #2	DP-I/O	PD 15k in US15W	-
A44	USB_2_3_OC#	USB Over current Pair 2 / 3	I-3.3	PU 10k 3.3V	-
A45	USB0-	USB Data- Port #0	DP-I/O	PD 15k in US15W	-
A46	USB0+	USB Data+ Port #0	DP-I/O	PD 15k in US15W	-
A47	VCC_RTC	RTC Power Supply +3V	PWR	-	-
A48	EXCDO_PERST#	PCI Express Card 0 Reset	0-3.3	-	-
A49	EXCDO_CPPE#	PCI Express Card 0 Request	I-3.3	PU 8k2 3.3V	-
A50	LPC_SERIRQ	LPC Serial Interrupt Request	IO-3.3	PU 10k 3.3V	-
A51	GND_6	Power Ground	PWR	-	-
A52	PCIE_TX5+	Not Connected	nc	-	not supported
A53	PCIE_TX5-	Not Connected	nc	-	not supported
A54	SDIO_D0 / GPIO	SDIO#0 Data0 / General Purpose Input 0	I/O-3.3 / I-3.3	PU 75k in US15W / PU 100k 3.3V	- / CPLD I/O
A55	PCIE_TX4+	Not Connected	nc	-	not supported
A56	PCIE_TX4-	Not Connected	nc	-	not supported
A57	GND_7	Power Ground	PWR	-	-
A58	PCIE_TX3+	Not Connected	nc	-	not supported
A59	PCIE_TX3-	Not Connected	nc	-	not supported
A60	GND_8	Power Ground	PWR	-	-
A61	PCIE_TX2+	Not Connected	nc	-	not supported
A62	PCIE_TX2-	Not Connected	nc	-	not supported
A63	SDIO_D1 / GPI1	SDIO#0 Data1 / General Purpose Input 1	I/O-3.3 / I-3.3	PU 75k in US15W / PU 100k 3.3V	- / CPLD I/O
A64	PCIE_TX1+	PCIe lane #1 Transmit+	DP-0	PU 50R inUS15W	only available on no-LAN var.
A65	PCIE_TX1-	PCIe lane #1 Transmit-	DP-0	PU 50R inUS15W	only available on no-LAN var.
A66	GND_9	Power Ground	PWR	-	-
A67	SDIO_D2 / GPI2	SDIO#0 Data2 / General Purpose Input 2	I/O-3.3 / I-3.3	PU 75k in US15W / PU 100k 3.3V	- / CPLD I/O
A68	PCIE_TX0+	PCIe lane #0 Transmit+	DP-0	PU 50R inUS15W	-
A69	PCIE_TX0-	PCIe lane #0 Transmit-	DP-0	PU 50R inUS15W	-
A70	GND_10	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS Channel A (positive)	DP-0	PU 50R inUS15W	-
A72	LVDS_A0-	LVDS Channel A (negative)	DP-0	PU 50R inUS15W	-
A73	LVDS_A1+	LVDS Channel A (positive)	DP-0	PU 50R inUS15W	-
A74	LVDS_A1-	LVDS Channel A (negative)	DP-0	PU 50R inUS15W	-

A75	LVDS_A2+	LVDS Channel A (positive)	DP-0	PU 50R inUS15W	-
A76	LVDS_A2-	LVDS Channel A (negative)	DP-0	PU 50R inUS15W	-
A77	LVDS_VDD_EN	LVDS Panel Power Control	0-3.3	PD 100k	-
A78	LVDS_A3+	LVDS Channel A (positive)	DP-0	PU 50R inUS15W	-
A79	LVDS_A3-	LVDS Channel A (negative)	DP-0	PU 50R inUS15W	-
A80	GND_11	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Channel A Clock+	DP-0	PU 50R inUS15W	-
A82	LVDS_A_CK-	LVDS Channel A Clock-	DP-0	PU 50R inUS15W	-
A83	LVDS_I2C_CK	LVDS I2C Clock (DDC)	IO-3.3	PU 10k 3.3V	-
A84	LVDS_I2C_DAT	LVDS I2C Data (DDC)	IO-3.3	PU 10k 3.3V	-
A85	SDIO_D3 / GPI3	SDIO# Data3 / General Purpose Input 3	I/O-3.3 / I-3.3	PU 75k in US15W / PU 100k 3.3V	- / CPLD I/O
A86	KBD_RST#	Keyboard Reset	I-5T	PU 1M 3.3V	not supported on CE 1.x.x
A87	KBD_A20GATE	A20 gate	I-5T	PU 10k 3.3V	-
A88	PCIE0_CK_REF+	PCIe Clock (positive)	DP-0	-	100MHz
A89	PCIE0_CK_REF-	PCIe Clock (negative)	DP-0	-	100MHz
A90	GND_12	Power Ground	PWR	-	-
A91	RSVD1	Reserved	nc	-	-
A92	RSVD2	Reserved	nc	-	-
A93	SDIO_Clk / GP00	SDIO#0 Clock / General Purpose Output 0	0-3.3 / 0-3.3	- / PD 100k	24/48MHz / CPLD I/O
A94	RSVD3	Reserved	nc	-	-
A95	RSVD4	Reserved	nc	-	-
A96	GND_13	Power Ground	PWR	-	-
A97	VCC_12V_1	12V VCC	PWR	-	-
A98	VCC_12V_2	12V VCC	PWR	-	-
A99	VCC_12V_3	12V VCC	PWR	-	-
A100	GND_14	Power Ground	PWR	-	-
A101	VCC_12V_4	12V VCC	PWR	-	-
A102	VCC_12V_5	12V VCC	PWR	-	-
A103	VCC_12V_6	12V VCC	PWR	-	-
A104	VCC_12V_7	12V VCC	PWR	-	-
A105	VCC_12V_8	12V VCC	PWR	-	-
A106	VCC_12V_9	12V VCC	PWR	-	-
A107	VCC_12V_10	12V VCC	PWR	-	-
A108	VCC_12V_11	12V VCC	PWR	-	-
A109	VCC_12V_12	12V VCC	PWR	-	-
A110	GND_15	Power Ground	PWR	-	-

3.10.3 Connector X1A Row B

Pin	Signal	Description	Type	Termination (CE 4.x.x)	Comment
B1	GND_16	Power Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC Frame Indicator	0-3.3	-	-
B4	LPC_A0	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B5	LPC_AD1	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B6	LPC_AD2	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B7	LPC_AD3	LPC Address / Data Bus	IO-3.3	PU 20k in US15W	-
B8	LPC_DRQ0#	Not Connected	nc	-	-
B9	LPC_DRQ1#	Not Connected	nc	-	-
B10	LPC_CLK	LPC Clock	0-3.3	-	up to 33MHz
B11	GND_17	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button Input	I-3.3	PU 1k 3.3V	active on rising edge
B13	SMB_CLK	SMBus Clock	0-3.3	PU 2k8 3.3V	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 2k8 3.3V	-
B15	SMB_ALERT#	SMBus Interrupt	IO-3.3	PU 5k 3.3V	-
B16	SATA1_TX+	Not Connected	nc	-	not supported
B17	SATA1_TX-	Not Connected	nc	-	not supported
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices.	0-3.3	-	CPLD I/O
B19	SATA1_RX+	Not Connected	nc	-	not supported
B20	SATA1_RX-	Not Connected	nc	-	not supported
B21	GND_18	Power Ground	PWR	-	-
B22	SATA3_TX+	Not Connected	nc	-	not supported
B23	SATA3_TX-	Not Connected	nc	-	not supported
B24	PWR_OK	Power OK from power supply	I-5T	PU 1M 3.3V	CPLD I/O
B25	SATA3_RX+	Not Connected	nc	-	not supported
B26	SATA3_RX-	Not Connected	nc	-	not supported
B27	WDT	Indicator for Watchdog Timeout	0-3.3	-	CPLD I/O
B28	AC_SDIN2	Not Connected	nc	-	not supported
B29	AC_SDIN1	Audio Codec Serial Data in 1	I-3.3	PD 22k in US15W	-
B30	AC_SDIN0	Audio Codec Serial Data in 0	I-3.3	PD 22k in US15W	-
B31	GND_19	Power Ground	PWR	-	-
B32	SPKR	Speaker Interface	0-3.3	-	-
B33	I2C_CLK	General Purpose I2C Clock	IO-3.3	PU 2k2 3.3V	CPLD I/O
B34	I2C_DAT	General Purpose I2C Data	IO-3.3	PU 2k2 3.3V	CPLD I/O
B35	THRM#	Over Temperature	I-3.3	-	CPLD I/O

		Indicator			
B36	USB7-	USB Data- Port #7 (USB Mode) / USB Data- Client (Client Mode)	DP-I/O / DP-I/O	PD 15k in US15W / PU 1k5 in US15W	- / -
B37	USB7+	USB Data+ Port #7 (USB Mode) / USB Data+ Client (Client Mode)	DP-I/O / DP-I/O	PD 15k in US15W / PU 1k5 in US15W	- / -
B38	USB_4_5_OC#	USB Over current Pair 4 / 5	I-3.3	PU 10k 3.3V	-
B39	USB5-	USB Data- Port #5	DP-I/O	PD 15k in US15W	-
B40	USB5+	USB Data+ Port #5	DP-I/O	PD 15k in US15W	-
B41	GND_20	Power Ground	PWR	-	-
B42	USB3-	USB Data- Port #3	DP-I/O	PD 15k in US15W	-
B43	USB3+	USB Data+ Port #3	DP-I/O	PD 15k in US15W	-
B44	USB_0_1_OC#	USB Over current Pair 0 / 1	I-3.3	PU 10k 3.3V	-
B45	USB1-	USB Data- Port #1	DP-I/O	PD 15k in US15W	-
B46	USB1+	USB Data+ Port #1	DP-I/O	PD 15k in US15W	-
B47	EXCD1_PERST#	PCIe Express Card 1 Reset	0-3.3	-	-
B48	EXCD1_CPPE#	PCIe Express Card 1 Request	I-3.3	PU 8k2 3.3V	-
B49	SYS_RESET#	Reset button input	I-3.3	PU 5k-25k in CPLD	-
B50	CB_RESET#	Carrier Board Reset	0-3.3	-	CPLD I/O
B51	GND_21	Power Ground	PWR	-	-
B52	PCIE_RX5+	Not Connected	nc	-	not supported
B53	PCIE_RX5-	Not Connected	nc	-	not supported
B54	SDIO_CMD / GP01	SDIO#0 Command / General Purpose Output 1	I/O-3.3 / 0-3.3	PU 75k 3.3V / PD 100k	- / CPLD I/O
B55	PCIE_RX4+	Not Connected	nc	-	not supported
B56	PCIE_RX4-	Not Connected	nc	-	not supported
B57	SDIO_WP / GP02	SDIO#0 Write Protection / General Purpose Output 2	I-3.3 / 0-3.3	PU 100k 3.3V / PD 100k	- / -
B58	PCIE_RX3+	Not Connected	nc	-	not supported
B59	PCIE_RX3-	Not Connected	nc	-	not supported
B60	GND_22	Power Ground	PWR	-	-
B61	PCIE_RX2+	Not Connected	nc	-	not supported
B62	PCIE_RX2-	Not Connected	nc	-	not supported
B63	SDIO_CD# / GP03	SDIO#0 CardDetect / General Purpose Output 3	I-3.3 / 0-3.3	PU 10k 3.3V / PD 100k	- / -
B64	PCIE_RX1+	PCIe lane #1 Receive+	DP-I	PD 50R inUS15W	only available on no-LAN var.
B65	PCIE_RX1-	PCIe lane #1 Receive-	DP-I	PD 50R inUS15W	only available on no-LAN var.
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 1k 3.3V	CPLD I/O
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 10k 3.3V	CPLD I/O
B68	PCIE_RX0+	PCIe lane #0 Receive+	DP-I	PD 50R inUS15W	-
B69	PCIE_RX0-	PCIe lane #0 Receive-	DP-I	PD 50R inUS15W	-
B70	GND_23	Power Ground	PWR	-	-

B71	LVDS_B0+	Not Connected	nc	-	not supported
B72	LVDS_B0-	Not Connected	nc	-	not supported
B73	LVDS_B1+	Not Connected	nc	-	not supported
B74	LVDS_B1-	Not Connected	nc	-	not supported
B75	LVDS_B2+	Not Connected	nc	-	not supported
B76	LVDS_B2-	Not Connected	nc	-	not supported
B77	LVDS_B3+	Not Connected	nc	-	not supported
B78	LVDS_B3-	Not Connected	nc	-	not supported
B79	LVDS_BKLT_EN	Backlight Enable	0-3.3	PD 100k	-
B80	GND_24	Power Ground	PWR	-	-
B81	LVDS_B_CK+	Not Connected	nc	-	not supported
B82	LVDS_B_CK-	Not Connected	nc	-	not supported
B83	LVDS_BKLT_CTRL	Backlight Brightness Control	0-3.3	-	-
B84	VCC_5V_SBY	+5V Standby	PWR	-	-
B85	VCC_5V_SBY	+5V Standby	PWR	-	-
B86	VCC_5V_SBY	+5V Standby	PWR	-	-
B87	VCC_5V_SBY	+5V Standby	PWR	-	-
B88	RSVD5	Reserved	-	-	-
B89	VGA_RED	Not Connected	nc	-	not supported
B90	GND_25	Power Ground	PWR	-	-
B91	VGA_GRN	Not Connected	nc	-	not supported
B92	VGA_BLU	Not Connected	nc	-	not supported
B93	VGA_HSYNC	Not Connected	nc	-	not supported
B94	VGA_VSYNC	Not Connected	nc	-	not supported
B95	VGA_I2C_CK	Not Connected	nc	-	not supported
B96	VGA_I2C_DAT	Not Connected	nc	-	not supported
B97	TV_DAC_A	Not Connected	nc	-	not supported
B98	TV_DAC_B	Not Connected	nc	-	not supported
B99	TV_DAC_C	Not Connected	nc	-	not supported
B100	GND_26	Power Ground	PWR	-	-
B101	VCC_12V_13	12V VCC	PWR	-	-
B102	VCC_12V_14	12V VCC	PWR	-	-
B103	VCC_12V_15	12V VCC	PWR	-	-
B104	VCC_12V_16	12V VCC	PWR	-	-
B105	VCC_12V_17	12V VCC	PWR	-	-
B106	VCC_12V_18	12V VCC	PWR	-	-
B107	VCC_12V_19	12V VCC	PWR	-	-
B108	VCC_12V_20	12V VCC	PWR	-	-
B109	VCC_12V_21	12V VCC	PWR	-	-
B110	GND_27	Power Ground	PWR	-	-



The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

3.10.4 SDVO Connector J1801 (optional)

With hardware revision CE 4.x.x or newer the nanoETExpress-SP provides an optional Serial DVO graphics output via onboard flat foil connector J1801.



Pin	Signal	Description	Type	Termination	Comment
1	GND#1	Ground	PWR	-	-
2	SDVOB_CLK_N	Serial Digital Video Channel B Clock-	DP-0	PU 50R inUS15W	-
3	SDVOB_CLK_P	Serial Digital Video Channel B Clock+	DP-0	PU 50R inUS15W	-
4	GND#2	Ground	PWR	-	-
5	SDVOB_GREEN_N	Serial Digital Video Channel B Green-	DP-0	PU 50R inUS15W	-
6	SDVOB_GREEN_P	Serial Digital Video Channel B Green+	DP-0	PU 50R inUS15W	-
7	GND#3	Ground	PWR	-	-
8	SDVOB_INT_N	Serial Digital Video Input Interrupt-	DP-I	PU 50R inUS15W	-
9	SDVOB_INT_P	Serial Digital Video Input Interrupt+	DP-I	PU 50R inUS15W	-
10	GND#4	Ground	PWR	-	-
11	SDVOB_BLUE_N	Serial Digital Video Channel B Blue-	DP-0	PU 50R inUS15W	-
12	SDVOB_BLUE_P	Serial Digital Video Channel B Blue+	DP-0	PU 50R inUS15W	-
13	GND#5	Ground	PWR	-	-
14	SDVOB_RED_N	Serial Digital Video Channel B Red-	DP-0	PU 50R inUS15W	-
15	SDVOB_RED_P	Serial Digital Video Channel B Red+	DP-0	PU 50R inUS15W	-
16	GND#6	Ground	PWR	-	-
17	SDVOB_STALL_N	Serial Digital Video Field Stall-	DP-I	PD 50R inUS15W	-
18	SDVOB_STALL_P	Serial Digital Video Field Stall+	DP-I	PD 50R inUS15W	-
19	GND#7	Ground	PWR	-	-
20	SDVO_CTRLCLK	SDVO Control Clock	DP-I/O	-	-
21	SDVO_CTRLDATA	SDVO Control DATA	DP-I/O	-	-
22	RESET#	Module Reset	-	-	-
23	VCC#1	V3.3_S0	PWR	-	-
24	VCC#2	V2.5_S0	PWR	-	-
25	VCC#3	V5.0_S0	PWR	-	-
26	GND#8	Ground	PWR	-	-
27	SDVOB_TVCLKIN_N	SDVO Channel B TV-Out Sync Clock-	DP-I	PD 50R inUS15W	-
28	SDVOB_TVCLKIN_P	SDVO Channel B TV-Out Sync Clock+	DP-I	PD 50R inUS15W	-
29	VCC#4	V3.3_S0	PWR	-	-
30	VCC#5	V5.0_S0	PWR	-	-

3.10.5 XDP Connector J1400 (optional)

The nanoETXexpress-SP provides the XDP debug port of Silverthorne CPU optionally with connector J1400.



The debug port is for internal use only. Do not connect any devices.

3.11 Signal Description

3.11.1 PCIexpress x1 lanes

The PCI express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® / COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

The nanoETXexpress-SP has 1 PCIe X1
2 PCIe X1 without LAN.

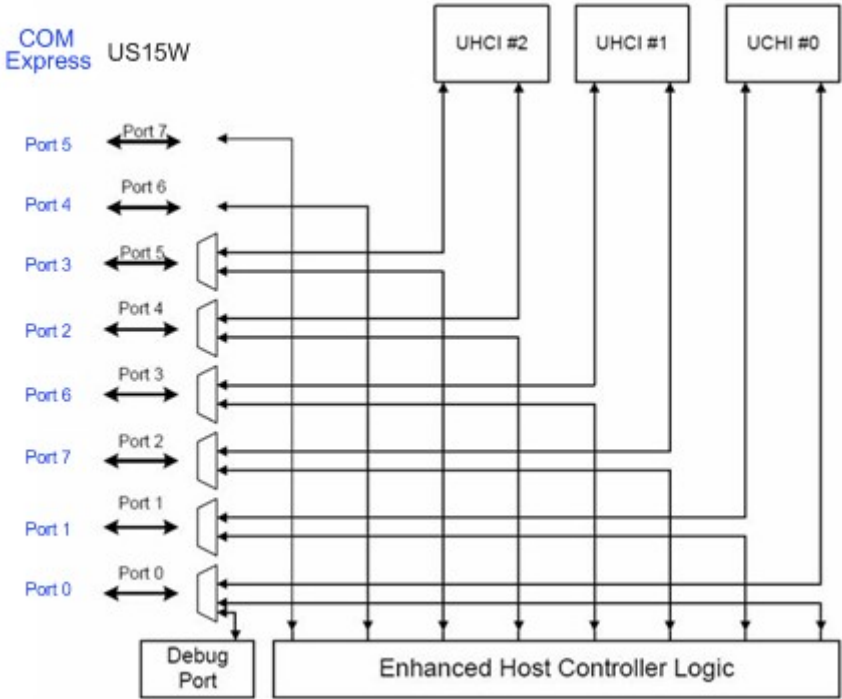
Only on nanoETXexpress-SP without LAN two PCIe x1 lanes are available and can be used for additional PCIe devices.

3.11.2 USB

The USB interface comes with three USB controllers (6 USB ports). The USB configuration of the nanoETXexpress-SP module is described in the following table:

COM Express Port	SCH US15W Port	Description
USB0	USB0	USB 2.0 compliant
USB1	USB1	USB 2.0 compliant
USB2	USB4	USB 2.0 compliant
USB3	USB5	USB 2.0 compliant
USB4	USB6	Not USB 2.0 compliant, no UHCI controller (no USB 1.1 / USB 2.0 only)
USB5	USB7	Not USB 2.0 compliant, no UHCI controller (no USB 1.1 / USB 2.0 only)
USB6	USB3	USB 2.0 compliant
USB7	USB2	USB Client or USB 2.0 compliant port (configurable in BIOS Setup)

Internal USB mapping from US15W SCH



The amount of available USB connections can be expanded by adding external USB-hubs.

USB Client Port

The USB interface supports also one USB client port (USB port 7) that can be activated in setup. If the client function is disabled in the BIOS this port acts as a normal USB 2.0 port. Please be aware that USB power lines may not be connected on the USB client port.



Special USB client and host driver software is needed for USB client function. When this driver and software is installed the client port appears as a mass storage device and NDIS Network device or as NDIS Network device only in the device manager of the operating system. Please refer to the Kontron download page for nanoETXexpress-SP for the driver

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

3.11.3 SATA

The nanoETXexpress-SP offers 1 x SATA 150 (SATA #0)

Marvell 88SA8052 PATAtoSATA (IDE Slave) ports to connect modern hard drive disks.

Following AHCI features are supported: NO

Following RAID Modes are supported: NO

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.



When using a hard disk on SATA #0 as primary device for the operating system the boot order should be changed according the usage. Wrong boot order may cause problems writing the MBR during OS installation.

3.11.4 Audio

The nanoETXexpress-SP has an HD Audio interface.



Baseboards with AC'97 codec only are not supported.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

3.11.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in “Continuous Mode”

3.11.6 Graphics Interface

The nanoETXexpress-SP uses the graphics accelerator GMA500 with 200MHz GPU clock integrated in the Intel® System Controller Hub (US15W), which delivers shader-based technologies and high-performance 2D, 3D and video capabilities. The GMA500 graphics engine supports a variety of LCD panels with single clock, color depths of 18/24 bit and resolutions up to WXGA (1366×768). The maximum supported pixelclock of the system controller hub is 112 MHz.

Hardware video decode acceleration relieves the decode burden from the processor and reduces the power consumption of the system. Full hardware acceleration of H.264, MPEG2, VC1 and WMV9 eliminates the need of a software codec and offloads the CPU.

The graphic adapter uses the onboard RAM as graphic memory. The preallocated memory is defined through bios settings.

Possible settings are:

- » 1MB
- » 4MB
- » 8MB

The total amount of graphics memory in the operating system depends on the size of system memory and the used driver settings. The graphics media accelerator driver GMA uses DVMT to manage allocating of system memory according to the needs of running applications. The Intel® Embedded Graphics Driver IEGD allocates the maximum of graphics memory depending on system memory and driver settings.

Physical Memory of nanoETXexpress-SP	Preallocated Memory in BIOS Setup	Maximum Graphics Memory with GMA Driver	Maximum Graphics Memory with IEGD
512MB	1MB	127MB	352MB
512MB	4MB	126MB	352MB
512MB	8MB	125MB	352MB
1024MB	1MB	255MB	352MB
1024MB	4MB	254MB	352MB
1024MB	8MB	253MB	352MB



For memory allocation according to the table above BIOS revision NOW1R112 or newer is recommended

When using 1MB Preallocated Memory an Operating Systems without active GMA or IEGD may have problems to display a screen (e.g. during WinXP installation).

VGA

The nanoETXexpress-SP graphics subsystem GMA500 integrated in the Intel® System Controller Hub US15W does not support VGA output.

LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide. Refer to the documentation for additional information.

SDVO

A Serial DVO connection is supported with hardware revision CE 4.x.x or newer. The digital display channel configured from display Pipe A in GMA500 graphics adapter is capable of driving SDVO adapters that provide interfaces to a variety of external display technologies such as HDMI, DVI, TV-out or CRT (the maximum supported pixel clock is 160MHz). Contact your local sales representative which adapters are available.

SDVO can be used optionally via onboard flat foil connector or project based on COM Express connector replacing unused second channel LVDS B and CRT pins.

Alternative COM Express Pin-out with SDVO option:

Pin	Standard Signal	SDVO Option	SDVO Option Pin Description	Type	SDVO Termination
B71	LVDS_B0+	SDVOB_RED_P	Serial Digital Video Channel B Red+	DP-0	PU 50R inUS15W
B72	LVDS_B0-	SDVOB_RED_N	Serial Digital Video Channel B Red-	DP-0	PU 50R inUS15W
B73	LVDS_B1+	SDVOB_GREEN_P	Serial Digital Video Channel B Green+	DP-0	PU 50R inUS15W
B74	LVDS_B1-	SDVOB_GREEN_N	Serial Digital Video Channel B Green-	DP-0	PU 50R inUS15W
B75	LVDS_B2+	SDVOB_BLUE_P	Serial Digital Video Channel B Blue+	DP-0	PU 50R inUS15W
B76	LVDS_B2-	SDVOB_BLUE_N	Serial Digital Video Channel B Blue-	DP-0	PU 50R inUS15W
B77	LVDS_B3+	SDVOB_INT_P	Serial Digital Video Input Interrupt+	DP-I	PD 50R inUS15W
B78	LVDS_B3-	SDVOB_INT_N	Serial Digital Video Input Interrupt-	DP-I	PD 50R inUS15W
B81	LVDS_B_CLK+	SDVOB_CLK_P	Serial Digital Video Channel B Clock+	DP-0	PU 50R inUS15W
B82	LVDS_B_CLK-	SDVOB_CLK_N	Serial Digital Video Channel B Clock-	DP-0	PU 50R inUS15W
B91	VGA_GRN	SDVOB_TVCLKIN_P	SDVO Channel B TV-Out Sync Clock+	DP-I	PD 50R inUS15W
B92	VGA_BLU	SDVOB_TVCLKIN_N	SDVO Channel B TV-Out Sync Clock-	DP-I	PD 50R inUS15W
B93	VGA_HSYNC	SDVOB_STALL_P	Serial Digital Video Field Stall+	DP-I	PD 50R inUS15W
B94	VGA_VSYNC	SDVOB_STALL_N	Serial Digital Video Field Stall-	DP-I	PD 50R inUS15W
B95	VGA_I2C_CLK	SDVO_CTRLCLK	SDVO Control Clock	DP-I/O	
B96	VGA_I2C_DAT	SDVO_CTRLDATA	SDVO Control DATA	DP-I/O	



The SDVO option is not available on a standard module. Please contact your local sales representative for more details or further questions.

3.11.7 Ethernet

The Ethernet interface offers 10/100/1000 Mbit connections and is driven by the Intel® 82574L (Hartwell). The device auto-negotiates the use of the different speed connections.

The ethernet interface operates at lowest power (<1W) when Gbit-Ethernet is fully active and supports functions as WOL (Wake On LAN), PXE (Preboot eXecution Environment) boot and Jumbo Frames.

For cable lengths and terminations on your baseboard please refer to the COM Express® Design Guide.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

3.11.8 LPC Bus

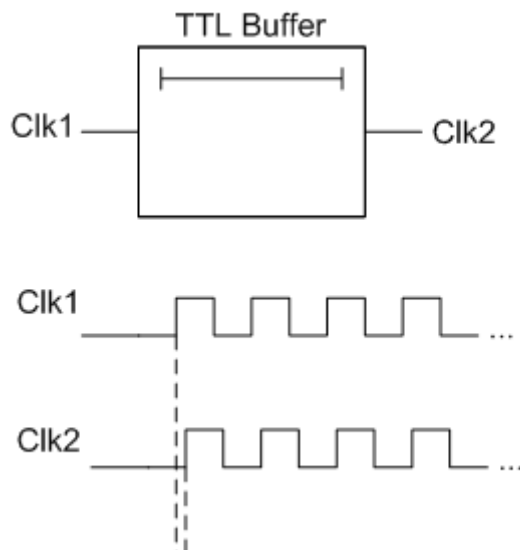
The Low Pin Count Interface signals are connected to the LPC Bus bridge, which is located in the Intel® US15W system controller hub. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the COM Express® Design Guide by PICMG. Refer to the documentation for additional information.

The LPC bus does not support DMA (Direct Memory Access). This leads to limitations for ISA bus and SIO (standard I/O's like Floppy or LPT interfaces) implementations. When more than one device is connected to the LPC bus a clock buffer is required!



Due to Power management of the LPC Bus, clock buffers that require synchronization should be used with great care and may prevent the board from booting up.

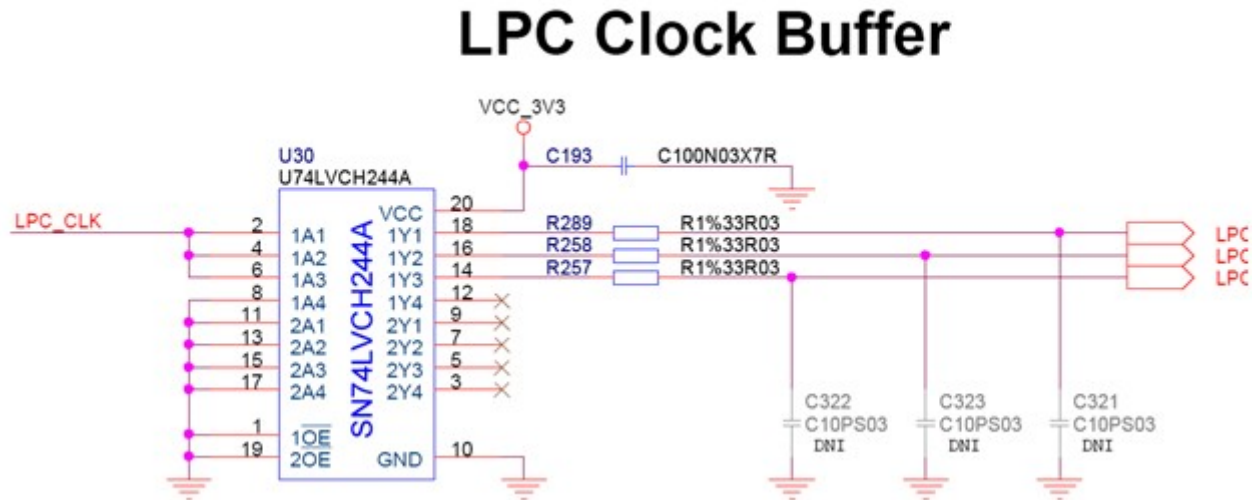
Standard Clock Buffer



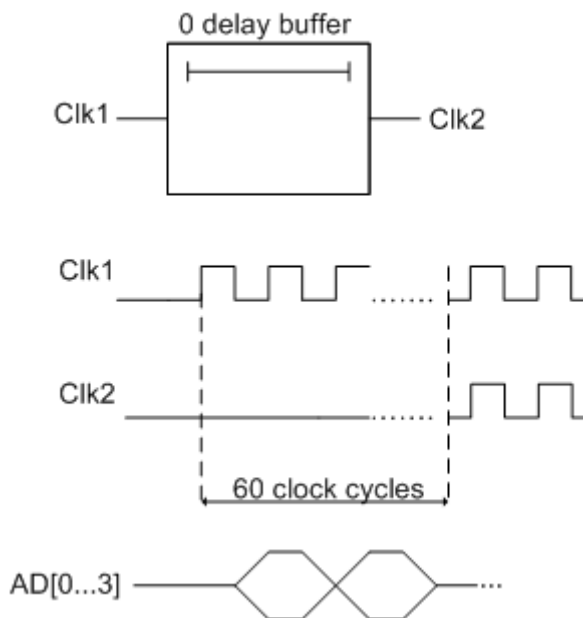
When using a standard clock buffer on the baseboard please be aware that the generated delay has to be considered for the length matching of the layout.

Clock Buffer Reference Schematic

The implementation of a clock buffer can be realized as shown in the evaluation schematic below:



Zero Delay Clock Buffer



Do not use the reference schematic in the COM Express™ Design Guide. Either use another Clock Buffer solution without a long start up process or use series resistors to double the LPC clock line. Follow the design recommendations in the COM Express Design Guide by PICMG.

3.11.9 Power Control

Power Supply

The nanoETXexpress-SP has a wide range power input from 4.75 - 14V. The supply voltage is applied through the VCC pins (VCC) of the module connector.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms ($50\text{ms} \leq t < 4\text{s}$) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Power Good (PWR_OK)

The nanoETXexpress-SP provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express™ Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded.

ATX Mode / Single Supply Mode

ATX Mode: By connecting an ATX power supply PWR_OK is set to low level and VCC is off. Press the Power Button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# via inversion.

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V → VCC
S0	high	high	5V	low	VCC

Single Supply Mode or automatic power on after power loss: In single supply mode the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V). PS_ON# is not used and V5_StdBy is not important (no difference if connected or not) in this mode.

To power on the module from S5 state press the power button or reconnect VCC

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	x	x	x	0
G3 → S0	high	open / high	x	connecting VCC
S5	high	open / high	x	VCC
S5 → S0	PWRBTN Event	open / high	x	reconnecting VCC



All columns marked with an “x” are not important for the specific power state.

All ground pins have to be tied to the ground plane of the carrier board.

3.11.10 Miscellaneous Circuits

Speaker

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the official PICMG documentation for additional information.

Battery

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the official documentation maintained by PICMG for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

For additional information, refer to the COM Express™ Design Guide, I2C application notes and JIDA specifications which are available at the [customer section](#) of Kontron's Website. See BIOS chapter for supported features and speed of I2C.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the -. The SMBus is a two wire bidirectional bus (clock and serial data) used for system management such as reading parameters from a memory card, and reading temperatures and voltages of system components. The SM Bus uses the same signaling scheme as an I2C bus.

4 Special Features

4.1 Watchdog Timer

This feature is implemented in the onboard CPLD. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API. The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- » 1-second increments from 1 to 255 seconds
- » 1-minute increments from 1 to 255 minutes

Contact Kontron Embedded Modules technical support for information on programming and operating the WDT.

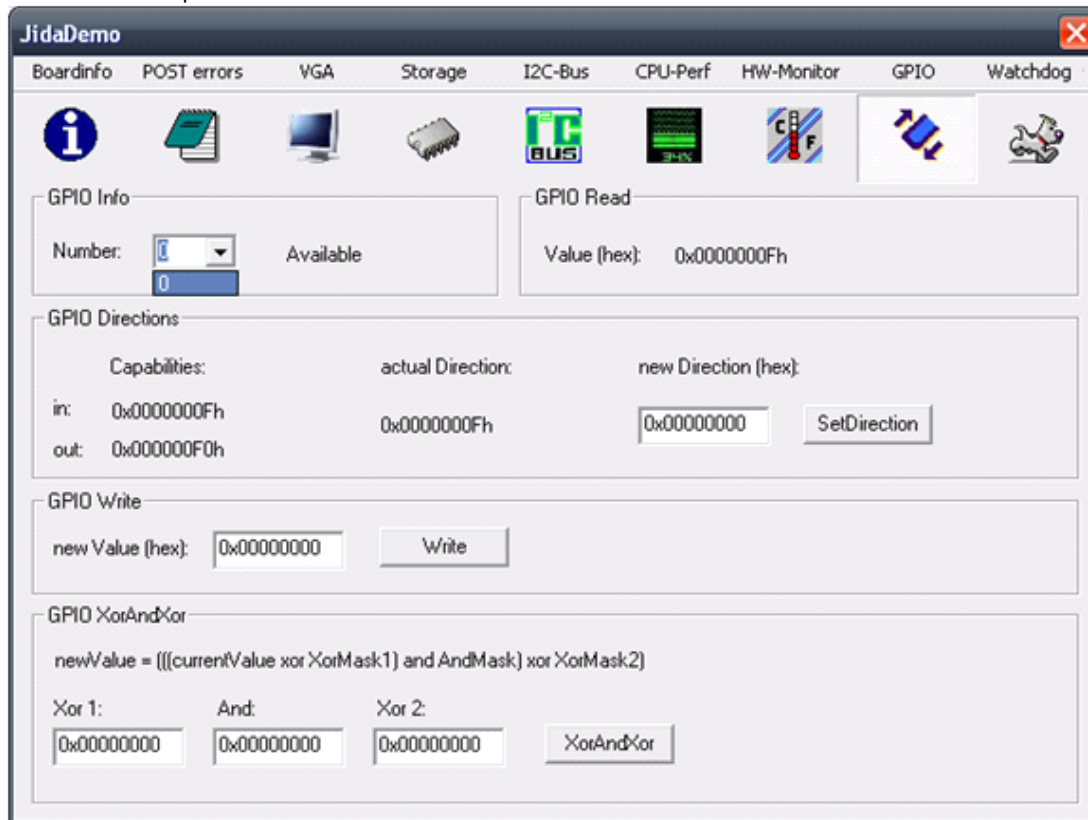
4.2 GPIO - General Purpose Input and Output

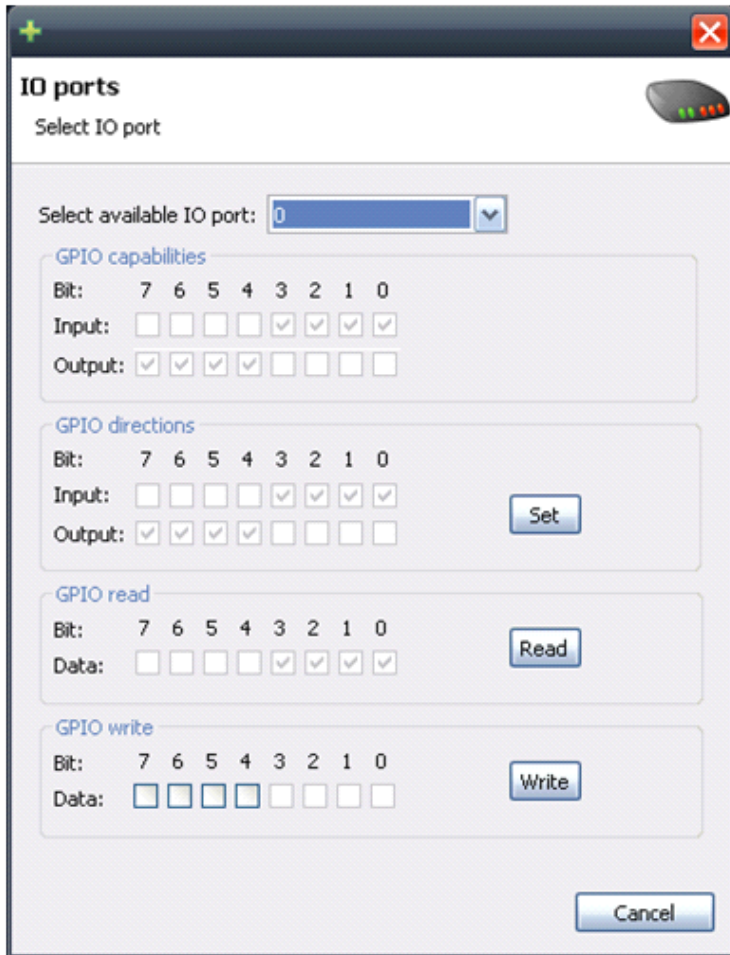
The nanoETXexpress-SP offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32/K-Station. Please refer to the JIDA32/K-Station manual in the driver download packet on our [customer section](#).





To enable GPIO functionality, modules with HW revision CE 1.x.x must be reworked. Contact your local sales or support for further information. On modules with HW revision CE 4.x.x and BIOS R115 or newer GPIO/SDIO can be switched via BIOS setup option

The General Purpose Inputs and Outputs are not applicable to drive applications faster than 2ms. It's recommended to use data transfer rates only up to 1 kHz.

General Purpose Outputs are high impedance until first write access

There is one IO Port controlled via onboard CPLD (1 Byte, Port 0) available and the 4 Inputs and 4 Outputs are fixed in direction. To access the GPIOs use the JIDA32 interface. You can write to a General Purpose Output with the upper half byte. To read a General purpose Input use the lower half byte.

Bit of GPIO Port0	Function	COM Express Pin
0	GPI0	A54
1	GPI1	A63
2	GPI2	A67
3	GPI3	A85
4	GPO0	A93
5	GPO1	B54
6	GPO2	B57
7	GPO3	B63

4.3 Speedstep Technology

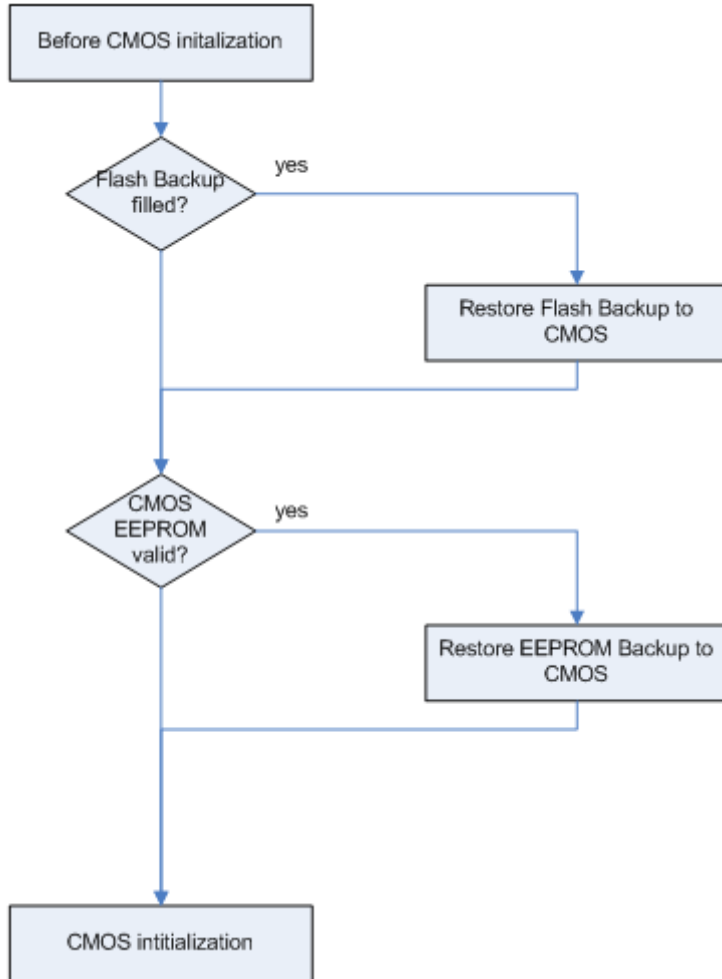
The Intel® processors offers the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It let you customize high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By disabling the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

4.4 Flash Backup Feature

The nanoETXexpress-SP supports a new functionality called “Flash Backup”. This new feature allows saving custom defaults directly into the Flash. With invalid EEPROM data or without a CMOS EEPROM, the module will start up with these custom defaults. It’s possible to save this BIOS with changed defaults to an image and flash it on other modules.



To create a BIOS with custom defaults:

- » Change your BIOS settings
- » Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)



Flash Backup should show “Enter new Password” first time saving custom defaults. If it is not possible to set a new password or entering a password shows an error message, please clean up CMOS data with DOS command: **jidacmos rtc /clean** (jidacmos utility is available at Kontron’s Customer Section)

- » Extract the BIOS including custom defaults with afudos or kflash utility for windows

Tool	Command
AFUDOS	<code>c:\>afudos.exe biosname.rom /O</code>
KFLASH	<code>c:\>kflash.exe backup biosname.rom</code>

Flash your BIOS with custom defaults: To flash a BIOS with customized defaults extracted like described above, use following options

Operating System	Command
Windows OS	<code>c:\>kflash.exe flash biosname.rom /bncr</code>
DOS	<code>c:\>afudos.exe biosname.rom /p /b /n /c</code> <code>c:\>jidacmos.exe eep /clean</code>



kflash.exe is a shell tool included in Kontron K-Station System Utility Package.

jidacmos utility is included in the BIOS download packages at Kontron's customer section.

4.5 Hyper Threading

Hyper Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PC´s. Hyper-Threading works by duplicating certain sections of the processor—those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two „logical“ processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always relies on the Operating System.



Hyper Threading is only supported on the Z530 (1.6 GHz) version of the nanoETXexpress-SP. Operating system images from the 1.1GHz (Z510) and 1.6Ghz (Z530) module may not be fully compatible. It's recommended to use separate images on hyperthreading and non-hyperthreading variant.

4.6 SD-card Interface (SDIO)

The SD card standard is a standard for removable memory storages designed and licensed by the SD Card Association (<http://sdcard.org>). The card form factor, electrical interface, and protocol are all part of the SD Card specification. The Intel® System Controller Hub US15W supports up to 3 SDIO interfaces. On nanoETXexpress-SP the first interface SDIO#0 (4-bit wide) is shared with the module GPIO signals. The integrated SDIO 1.1/MMC 4.1 controller in US15W only supports byte-address mode for SDIO storage cards up to 2GB. Sector-addressing and SDHC is not supported.

» MMC 4.1 transfer rates can be up to 48MHz and bus widths of 1, 4 or 8 bits

» SDIO 1.1 supports transfer rates up to 24MHz and bus widths of 1 or 4 bits

The following table shows which GPIO-ports can be used for the SD-card interface:

General purpose Input/output	SD card interface signals
GPIO	SLOT0_DATA0
GPI1	SLOT0_DATA1
GPI2	SLOT0_DATA2
GPI3	SLOT0_DATA3
GPO0	SLOT0_CLK
GPO1	SLOT0_CMD
GPO2	SLOT0_WP
GPO3	SLOT0_CD#



The SD_CMD line needs a pull-up resistor that can vary depending on the length of the electrical paths (typical from 10kOhm to 100kOhm).

The maximum length for SDIO signals on the baseboard should be 80mm

SDIO boot is supported with BIOS NOW1R113 or newer for standard SD/MMC Cards on baseboards following the maximum length specification for SDIO (80mm).

4.7 Fast I2C

The nanoETXexpress-SP integrates two configurable I2C buses. The external I2C provided via US15W GPIOs on COM Express™ Connector Pin B33/B34, the LVDS I2C from US15W SCH is available on COM express™ connector pin A83/A84. The I2C interface offers full MultiMaster and Clock Stretching support. Fast I2C clock speed depends on the CPU performance and differs between ATOM™ Z510 and ATOM™ Z530 modules. See the tables below for measured values on nanoETXexpress-SP with BIOS NOW1R113.

JIDA/external I2C speed

Setup	ATOM™ Z510	ATOM™ Z530
Extra high	not supported	not supported
Very high	150 kHz	210 kHz
High	80 kHz	110 kHz
Medium	40 kHz	60 kHz
Slow	11 kHz	16 kHz
Very slow	1.5 kHz	2 kHz
Ultra slow	0.8 kHz	1 kHz

JILI I2C speed

Setup	ATOM™ Z510	ATOM™ Z530
Extra high	not supported	not supported
Very high	90 kHz	125 kHz
High	36 kHz	50 kHz
Medium	18 kHz	25 kHz
Slow	2.8 kHz	4 kHz
Very slow	1.0 kHz	1.3 kHz
Ultra slow	not supported	not supported

4.8 ACPI Suspend Modes and Resume Events

The nanoETXexpress-SP only supports the S3 state (=Save to Ram). S4 (=Save to Disk) is not supported by the BIOS (S4_BIOS) but S4_OS is supported by the following operating systems:

- » Windows XP
- » Windows Vista
- » Windows 7

The following events resume the system from S3:

- » USB Keyboard (1)
- » USB Mouse (1)
- » Power Button
- » WakeOnLan (2)

The following events resume the system from S4:

- » Power Button

The following events resume the system from S5:

- » Power Button
- » WakeOnLan (2)



(1) OS must support wake up via USB devices and baseboard must power the USB Port with StBy-Voltage

(2) WakeOnLan must be enabled in the driver options

5 Design Consideration

5.1.1 Thermal Management

A heatspreader plate assembly is available from Kontron Embedded Modules for the nanoETXexpress-SP. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express™-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components on the nanoETXexpress-SP. About 80 percent of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express™ application and environmental conditions. Please see the COM Express™ Design Guide for further information on thermal management.

5.1.2 Heatspreader

Documentation of nanoETXexpress-SP heatspreader and cooling solutions is provided at <http://emdcustomersection.kontron.com>.

6 System Resources

6.1 Interrupt Request (IRQ) Lines

Please be aware that an ACPI OS decides itself on resource usage. The tables below show only an example distribution.

6.1.1 In 8259 PIC Mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)



1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

6.1.2 In APIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + US15W graphics + USB UHCI Controller #1; Note (2)
17	PIRQ[B]	For PCI	PCI IRQ line 2 + LAN Controller + USB UHCI Controller #2; Note (2)
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UHCI Controller #3; Note (2)
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UHCI Controller #3; Note (2)
20	PIRQ[E]	No	Note (2)
21	PIRQ[F]	No	Note (2)
22	PIRQ[G]	No	Note (2)
23	PIRQ[H]	No	Note (2)



1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

2 ACPI Operating System decides on particular IRQ usage.

6.2 Memory Area

The first 640 kB of DRAM are used as main memory. Using DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available
A0000h – BFFFFh	VGA Memory	No
C0000h – CFFFFh	VGA BIOS	No
D0000h – DFFFFh		Yes
E0000h – FFFFFh	System BIOS	No

6.3 I/O Address Map

I/O Address	Used for	Available	Comment
0000 - 001F	System Resources	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
0040 - 005F	Timer, Counter	No	Fixed
0060 - 006F	Keyboard controller	No	Fixed
0070 - 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed
0084 - 008F	DMA Page Register	No	Fixed
0090 - 009F	System Control	No	Fixed
00A0 - 00BF	Interrupt Controller 2	No	Fixed
00E0 - 00EF	System Control	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
0170 – 0177; 0376	Fixed Disk	No	Available if IDE port 1 is disabled
01F0 - 01F7; 03F6	Fixed Disk	No	Available if IDE port 1 is disabled
274 - 279	PnP Port	No	Fixed
03B0 - 03DF	VGA	No	Fixed
0400 - 043F	Chipset	No	Fixed
0480 - 04BF	Chipset	No	Fixed
04D0 - 04D1	Chipset	No	Fixed
0900 - 091F	Power Management	No	Fixed
09C0 - 09FF	GPE	No	Fixed
0A05 – 0A06	WB83627HG Hardware Monitor	No	Fixed if WB83627HG is in system
0A80 – 0A81	CPLD	No	Fixed
0CF8 - 0CFF	PCI Configuration	No	Fixed
D880 - D887	PCI LAN Controller	No	Dynamic (BIOS default address)
E080 - E09F	PCI USB Controller	No	Dynamic (BIOS default address)
E480 - E49F	PCI USB Controller	No	Dynamic (BIOS default address)
E880 - E887	VGA	No	Dynamic (BIOS default address)
EF00 - EF1F	PCI USB Controller	No	Dynamic (BIOS default address)
FFA0 - FFAF	PCI IDE Controller	No	Dynamic (BIOS default address)

6.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) respectively the PCI Express Base 1.0a specification. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

PCI Device	PCI IRQ	Interface	Comment
Host Bridge / Memory Controller	None		Integrated in chipset
Graphics / Video Controller	INTA		Integrated in chipset
USB Client Controller	INTA		Integrated in chipset
HD Audio Controller	INTA		Integrated in chipset
PCI Express Port (Bridge)	INTA		Integrated in chipset
PCI Express Port (Bridge)	INTB		Integrated in chipset
UHCI USB Controller 1	INTA		Integrated in chipset
UHCI USB Controller 2	INTB		Integrated in chipset
UHCI USB Controller 3	INTC		Integrated in chipset
EHCI USB Controller	INTD		Integrated in chipset
SDIO/MMC Controller 1	INTA		Integrated in chipset
ISA Bridge / LPC Controller	None		Integrated in chipset
IDE Controller	None		Integrated in chipset
Network Controller	INTA	PCI Express	External i82574

6.5 Internal I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS Data	0
A2h	JIDA-EEPROM	No	EEPROM for CMOS Data	0

6.6 JILI I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	3
62h	MAX6253	No	DAC for Backlight brightness	3

6.7 SDVO I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
				2

6.8 System Management (SM) Bus

nanoETXexpress-SP module:

I2C Address	Used For	Comment	JIDA Bus Nr.
30h/60h	STTS424E02 Temp Sensor / SPD		1
98h	Winbond W83L771W HWM		1
A0h	SPD		1
A2h	SPD		1
D2h	Clockgenerator		1

Additional resources if connected to nanoETXexpress Evaluation Backplane and MARS

I2C Address	Used For	Comment	JIDA Bus Nr.
12h	SMART_Charger	Only be used by a SMB Charger	1
14h	SMART_Selector	Only be used by a SMB Selector	1
16h	SMART_Battery	Only be used by a SMB Battery	1
7Eh	PLX PEX8606AA PCIe Switch		1
DCh	ICS9DB8801C PCIe Clock Buffer		1

6.9 K-Station / JIDA32 resources

6.9.1 I2C

BUS	Function
I2C 0	External / JIDA I2C
I2C 1	SM-Bus
I2C 2	SDVO DDC
I2C 3	JILI DDC

6.9.2 Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)

6.9.3 GPIO

Port	Function
IO-Port 0	GPIO Port, Bit 0-3: Input, Bit 4-7: Output Direction Change possible with NOW1R117 and CE 4.6.0 or newer

6.9.4 Hardware Monitor

Sensor	Function
Temp 0	Module Temperature (internal IC temperature of onboard Winbond W839771 HWM)
Temp 1	CPU ACPI Temperature (measured with Winbond W839771 HWM))
Temp 2	External SIO Winbond 83627 Temp Sensor 1)
Temp 3	External SIO Winbond 83627 Temp Sensor 2
Temp 4	External SIO Winbond 83627 Temp Sensor 3
FAN 0	External carrier board SIO Winbond 83627 FAN Sensor 0
FAN 1	External carrier board SIO Winbond 83627 FAN Sensor 1
FAN 2	External carrier board SIO Winbond 83627 FAN Sensor 2
Voltage 0	External SIO Winbond 83627 Voltage Sensor 0: CoreA
Voltage 1	External SIO Winbond 83627 Voltage Sensor 1: CoreB
Voltage 2	External SIO Winbond 83627 Voltage Sensor 2: 3.3V Battery
Voltage 3	External SIO Winbond 83627 Voltage Sensor 3: +3.3V
Voltage 4	External SIO Winbond 83627 Voltage Sensor 4: +5V
Voltage 5	external SIO Winbond 83627 standby Voltage Sensor 5: +5V_SB
Voltage 6	external SIO Winbond 83627 standby Voltage Sensor 6: +12V
Voltage 7	external SIO Winbond 83627 standby Voltage Sensor 5: -5V
Voltage 8	external SIO Winbond 83627 standby Voltage Sensor 5: -12V

7 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

7.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

- » AMIBIOS © 2006 American Megatrends, Inc.
- » BIOS Date: 05/11710 15:07:00 Ver: 08.00.15
- » Kontron® BIOS Version <NOW1RXXX
- » Copyright 2002-2010 Kontron Embedded Modules GmbH

7.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.



Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

7.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press when the following string appears during bootup.

Press to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▶) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

7.3 BIOS Setup

7.3.1 Main Menu

```

BIOS SETUP UTILITY
Main  Advanced  PCIPnP  Boot  Security  Chipset  Exit
-----
System Overview
-----
Bios Info
Bios Version      : NOW1R117
AMI Core8 Version : 08.00.16
Build Date       : 08/25/10

▶ Module Info

System Time           [02:02:24]
System Date           [Tue 01/01/2002]

Displays Module Info

←  Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1  General Help
F10 Save and Exit
ESC  Exit

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```

Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

7.3.2 Module Info

Module Info	
Main Module Info Board Name : nanoETXexpress-SP Board Class : CPU Serial Number : NOW1NCD3S1006 Manufacturing Date : 5/22/2009 Hardware Revision : 5.0 Boot Counter : 11724 Processor Intel(R) Atom(TM) CPU Z530 @ 1.60GHz Speed : 1600 MHz Count : 1 System Memory Size : 507 MB ▶ Module Component Steppings ▶ Module Software Revisions ▶ Current Memory Configuration ▶ Current LUDS Configuration	Displays Module Component Steppings ← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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Module Component Steppings

Module Info	
Main Module Component Steppings CPU Stepping : <0x3272CA> C0 NB Stepping : <0x07> D2 SB Stepping : <0x07> D2 WD CPLD Revision : 0x16	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
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Module Software Revisions

Module Info	
Main	
Module Software Revisions Bios Version : NOW1R117 Bios Build ID : 117 CPU Microcode Rev : 23<0x17> CMC Module : Lo-0D2.026x Hi-0D2.018x GBE OPROM Version : 1.3.24 JIDA32 Handler Revision : 1.3.37 Loader Revision : 1.1 JDA Revision : 1.11 UBIOS Revision : 0016 JILI Core Revision : 1.2.1 JRC Revision : 132	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
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Memory Module Information

Module Info	
Main	
Module Software Revisions Bios Version : NOW1R116 Bios Build ID : 116 CPU Microcode Rev : 17<0x11> CMC Module : Lo-0D2.026x Hi-0D2.018x GBE OPROM Version : 1.3.24 JIDA32 Handler Revision : 1.3.32 Loader Revision : 1.1 JDA Revision : 1.11 UBIOS Revision : 0016 JILI Core Revision : 1.2.1 JRC Revision : 132	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
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Slot 1

Main	
SLOT 1	
Technology	: DDR2 SDRAM
Manufacturer	: Micron Technology
DRAM Manufacture	:
Manufacture Loc	: 00
Manufacture Rev	: 0000
Partnum	: 8xMT47H64M16HR-3
S/N	: 00000000
Manufacture Date	: N/A
Capacity	: 1024Mb
Frequency	: DDR2-667, PC2-5300 333Mhz
SPD Revision	: 1.0
Checksum	: UALID
	← Select Screen
	↑↓ Select Item
	F1 General Help
	F10 Save and Exit
	ESC Exit
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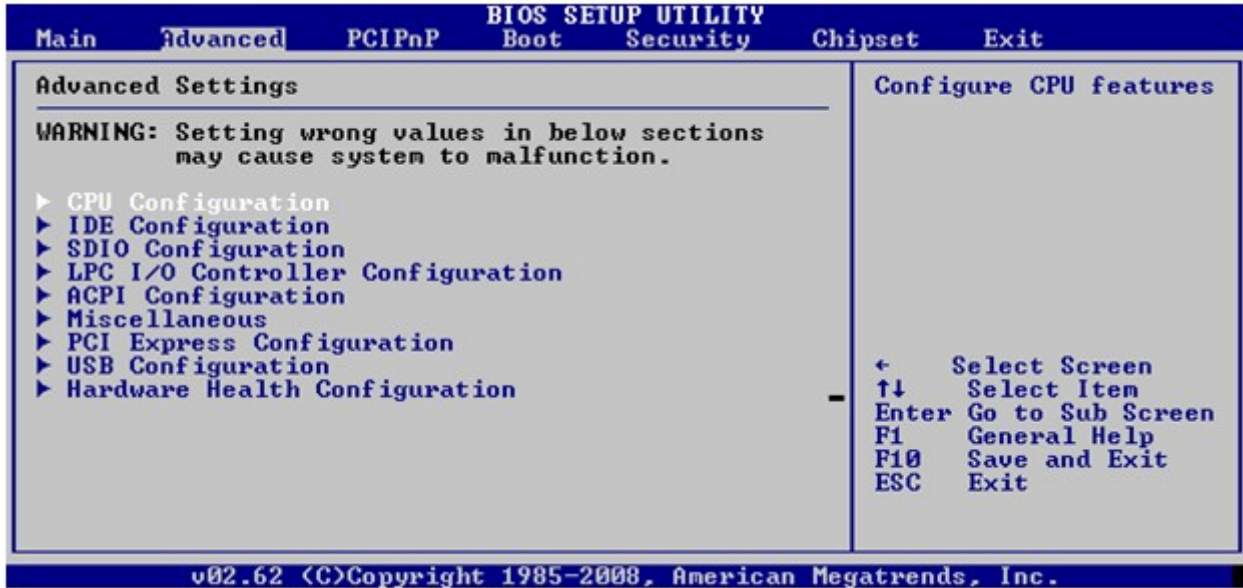


Current Memory Configuration SLOT1 shows information of onboard system memory stored in SPD. The SPD EEPROM is supported with CE 4.x.x (PCB L140) or newer.

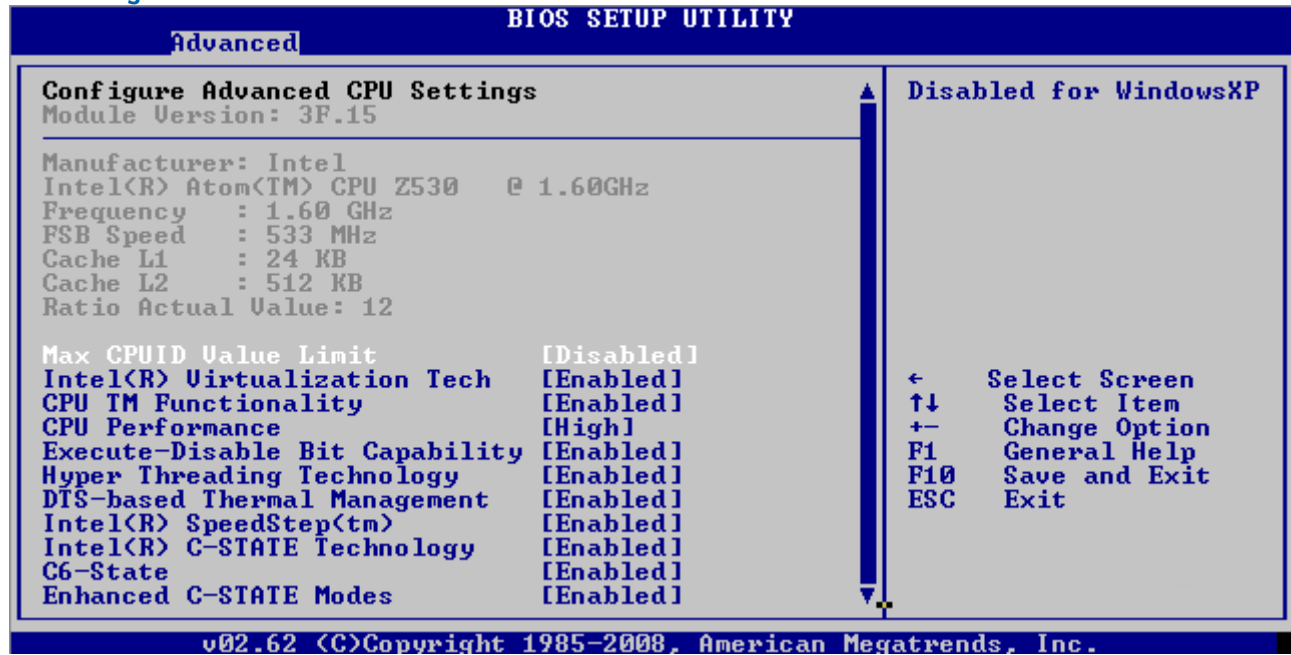
Current LVDS Configuration

Main	
Current LVDS Configuration	
Data Source	: LVDS - DUI ID
Resolution	: 1024x768
Color Depth	: 24Bit
Channel Count	: Single Channel
Dithering	: Disabled
	← Select Screen
	↑↓ Select Item
	F1 General Help
	F10 Save and Exit
	ESC Exit
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7.3.3 Advanced Menu



CPU Configuration



Feature	Option	Description
Max CPUID Value Limit	Disabled Enabled	Disabled for WindowsXP
Intel® Virtualization Tech	Enabled Disabled	When enabled, a VMM can utilize the additional HW Caps, provided by Intel® Virtualization Tech. Note: A full reset is required to change the setting.
CPU TM Functionality	Enabled Disabled	Enables or disables both TM1 and TM2 simultaneously.
CPU Performance	Low Middle High	Sets the CPU ratio for Z510/Z530 CPU Low: 600MHz / 800MHz Middle: 800MHz / 1200MHz High: 1100MHz / 1600MHz Note: Disable Speedstep to use fixed CPU speed to the selected performance state. With BIOS NOW1R113 or newer EIST is automatically disabled if set to low or middle.
Execute-Disable Bit Capability	Enabled Disabled	When disabled, force the XD feature flag to always return 0
Hyper Threading Technology	Enabled Disabled	Enable/Disable Intel® Hyper Threading Technology
DTS-based Thermal Management	Enabled Disabled	Enable/Disable Thermal Management utilizing the CPU's Digital Thermal Sensor
Intel® SpeedStep™	Enabled Disabled	Enables and Disables the SpeedStep power management feature
Intel® C-State Technology	Enabled Disabled	Enables and Disables the C - States. If enabled, the CPU is set to C2 - C4 state in idle mode
C6 state	Enabled Disabled	Enables and Disables the C6 - State.
Enhanced C-State Modes	Enabled Disabled	CPU idle is set to enhanced C-states, when enabled

IDE Configuration

Advanced		BIOS SETUP UTILITY
IDE Configuration		Enables or disables the IDE interface
IDE Controller	[Enabled]	
▶ IDE Master	: [Hard Disk]	
▶ IDE Slave	: [Not Detected]	
Hard Disk Write Protect	[Disabled]	
IDE Detect Time Out (Sec.)	[35]	
		← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
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Feature	Option	Description
IDE Controller	Enabled Disabled	Enables or disables the IDE interface of US15W SCH. This concerns the onboard SSD and PATA2SATA bridge.
Hard Disk Write Protect	Disabled Enabled	Disables/enables device write protection. It will be effective only if device is accessed through BIOS functions.
IDE Detect Time Out (Sec.)	[0-35] 35	Selects the time out value for the detection of ATA/ ATAPI devices

IDE Device Submenu



Feature	Option	Description
Type	Not Installed Auto CD/DVD ARMD	Selects the type of the IDE Devices connected to the system
LBA/Large Mode	Disabled Auto	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: The data transfer from and to the device occurs one sector at a time Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it
PIO Mode	Auto 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	Auto SWDMA MWDMA UDMA	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	Auto Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	Enabled Disabled	Disables and Enables the 32Bit Data Transfer Mode

AHCI Configuration

BIOS SETUP UTILITY

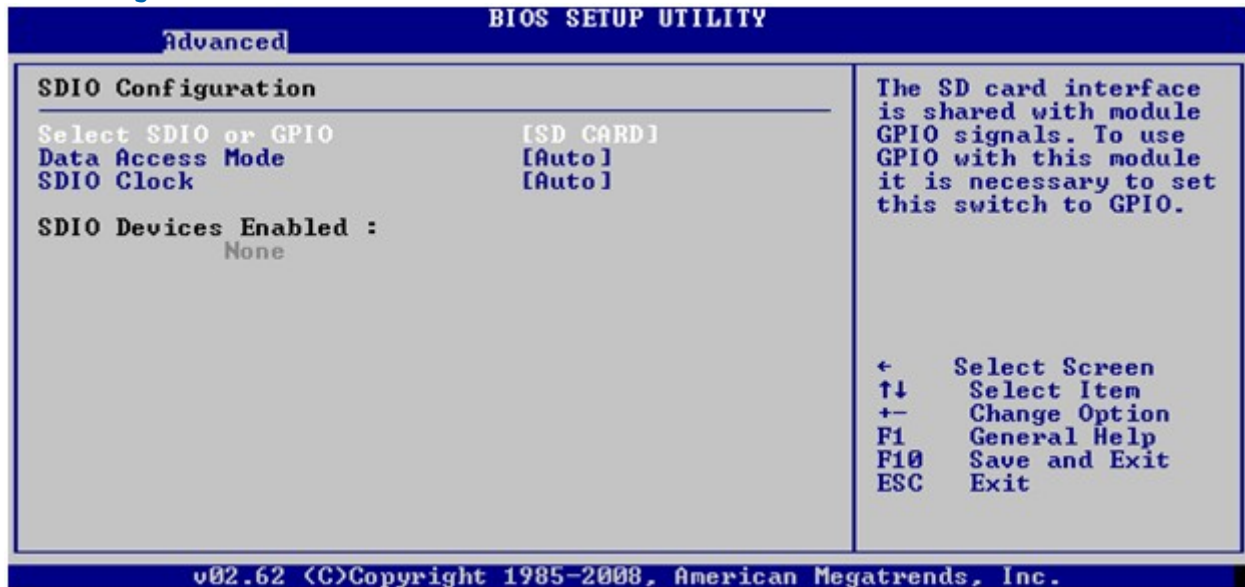
Advanced

AHCI Configuration	Enables for supporting
AHCI BIOS Support [Enabled]	
AHCI CD/DVD Boot Time out [35]	
▶ AHCI Port0 [Not Detected]	
▶ AHCI Port1 [Not Detected]	
▶ AHCI Port4 [Not Detected]	
▶ AHCI Port5 [Not Detected]	
	← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

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Feature	Option	Description
AHCI BIOS Support	Enabled Disabled	Enables / Disables the AHCI Support in BIOS
AHCI CD/DVD Boot Time out	0 5 10 ... 35	Selects the boot time out for AHCI CD/DVD devices

SDIO Configuration



Feature	Option	Description
Select SDIO or GPIO	SD Card GPIO	The SD card interface is shared with module GPIO signals. To use GPIO with this module it is necessary to set this switch to GPIO.
Data Access Mode	Auto DMA PIO	Auto: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA: Access SD device in DMA mode. PIO: Access SD device in PIO mode.
SDIO Clock	Auto 24 MHz	Limit SDIO Clock to 24MHz. Auto setting enables 48MHz clock if supported by the SDIO device.



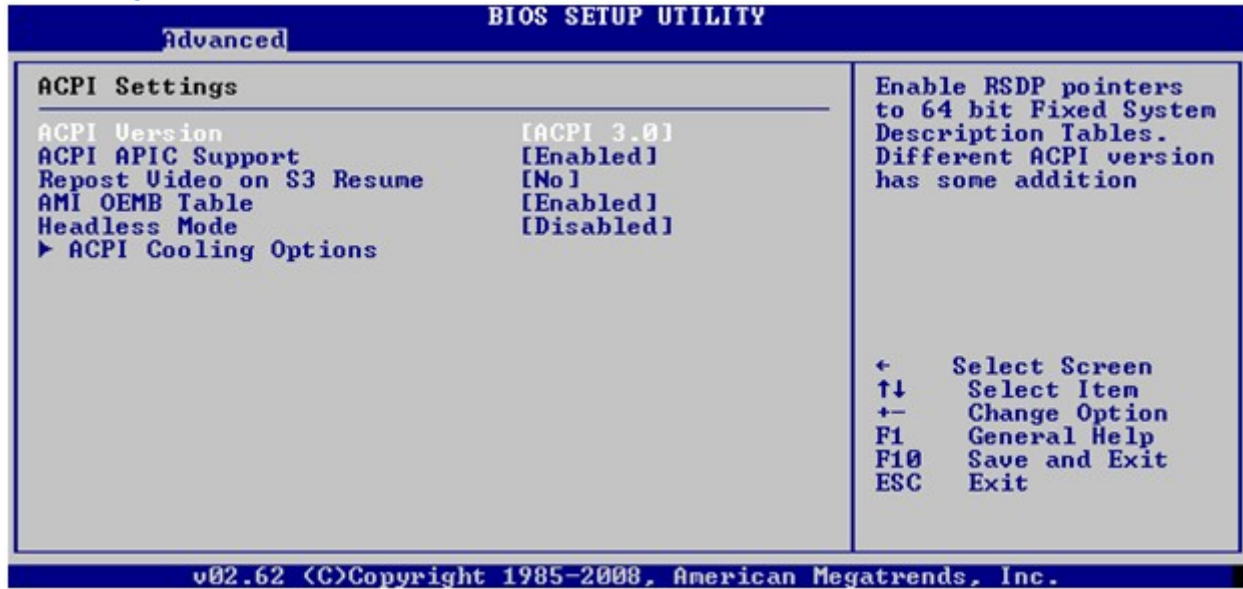
The SDIO/GPIO switch is only supported on hardware revisions CE 4.x.x or newer. Modules with revision CE 1.x.x must be reworked to enable GPIO functionality.

LPC I/O Controller Configuration

Advanced		BIOS SETUP UTILITY
Configure LPC I/O		Selects the serial Port1 base address
Serial Port1 Address	[3F8/IRQ4]	
Serial Port2 Address	[2F8/IRQ3]	
Serial Port2 Mode	[Normal]	
Parallel Port Address	[378]	
Parallel Port Mode	[Normal]	
Parallel Port IRQ	[IRQ7]	
		← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
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Feature	Option	Description
Serial Port1 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 1
Serial Port2 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 2
Serial Port2 Mode	Normal IrDA ASKIR	Selects the mode for serial Port 2
Parallel Port Address	Disabled 378 278 3BC	Selects the Address of the LPT Port
Parallel Port Mode	Normal Bi-Directional ECP EPP ECP+SPP	Allows BIOS to Select Parallel Port Mode. (Only visible when Parallel Port enabled.)
Parallel Port IRQ	IRQ5 IRQ7	Allows BIOS to Select Parallel Port IRQ. (Only visible when Parallel Port enabled.)

ACPI Configuration



Feature	Option	Description
ACPI Version	ACPI v.3.0 ACPI v.2.0	Selects the ACPI version
ACPI APIC support	Enabled Disabled	Include ACPI APIC table pointer to RSDT pointer list.
Repost Video on S3 Resume	No Yes	If yes, Videobios is reinitialized after S3 Resume
AMI OEMB Table	Enabled Disabled	Includes the AMI OEMB table pointer. The OEMB table is used to fill in POST data in AML code during ACPI OS operations. This option should only be disabled if ACPI 1.0 is used
Headless Mode	Disabled Enabled	Enables / Disables headless mode through ACPI

ACPI Cooling Options



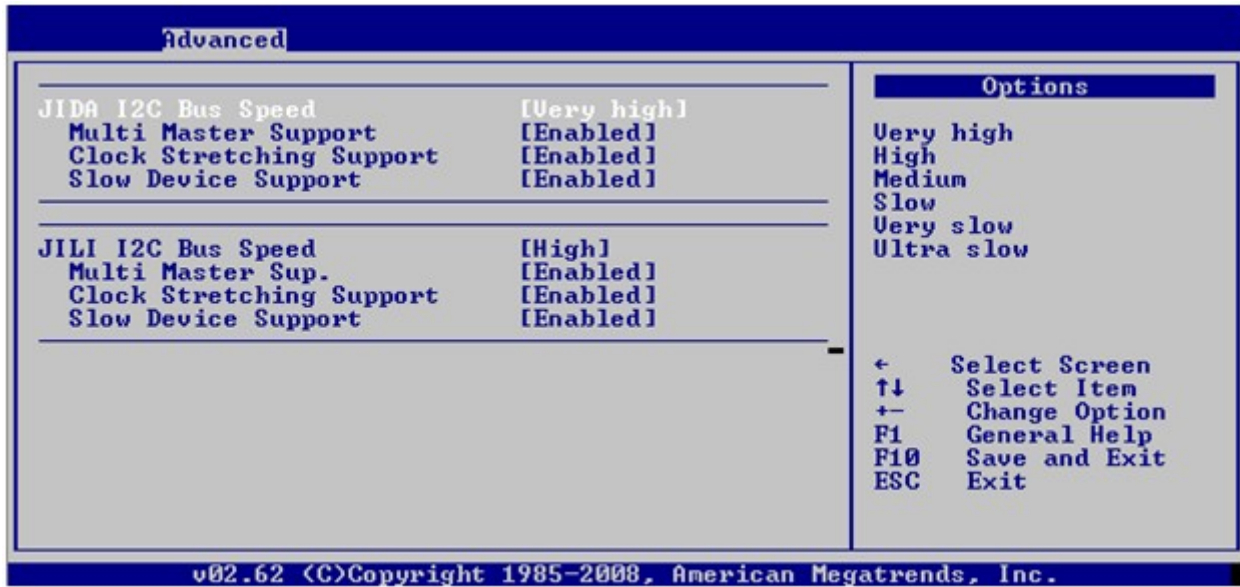
Feature	Option	Description
Passive Trip Point	Disabled 40°C 45°C 50°C ... 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
Passive TC1 value	1 2 3 ... 16	This value sets the TC1 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TC2 value	1 2 ... 5 ... 16	This value sets the TC2 value for the ACPI Passive Cooling Formula. (Only visible when Passive Trip Point is enabled.)
Passive TSP value	2 4 ... 10 ... 30	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point	Disabled 40°C 45°C 50°C ... 110°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut off the system.

Miscellaneous Settings



Feature	Option	Description
Spread Spectrum	Disabled LVDS Core Both	Enables or Disables spread spectrum for the selected Clocks. LVDS: Enables LVDS Spread Spectrum Core: Enables CPU, PCIe, Chipset Spread Spectrum
A20 line controlled by	Auto Detection Legacy Keyb Ctrl. Port 92h emul	This setting allows choosing how address line A20 is controlled for legacy systems. If Keyb. controller is chosen an active KBC is needed
Keyboard Crisis Recovery	Disabled Enabled	Enables/Disables Keyboard Crisis Recovery function by USB keyboard
Smbios Smi Support	Enabled Disabled	SM BIOS SMI Wrapper support for PnP Functions 50h-54h

I2C Busses



Feature	Option	Description
JIDA I2C Bus Speed	Very high High Medium ... Ultra Slow	Select speed for JIDA/external I2C bus. See table below for speed settings.
Multi Master support	Enabled Disabled	Enables / disables I2C multi master support
Clock Stretching support	Enabled Disabled	Enables / disables I2C clock stretching support
Slow Device support	Enabled Disabled	Enables / disables I2C clock stretching support
JILI I2C Bus Speed	Very high High Medium ... Ultra Slow	Select speed for JIDA/external I2C bus. See table below for speed settings.
Multi Master support	Enabled Disabled	Enables / disables I2C multi master support
Clock Stretching support	Enabled Disabled	Enables / disables I2C clock stretching support
Slow Device support	Enabled Disabled	Enables / disables I2C clock stretching support

Watchdog



Feature	Option	Description
Mode	Reset Disabled	Selects the mode of the watchdog
Timeout	1s 5s 10s 30s 1:00m 5:00m 10:00m	Set the timeout for Watchdog

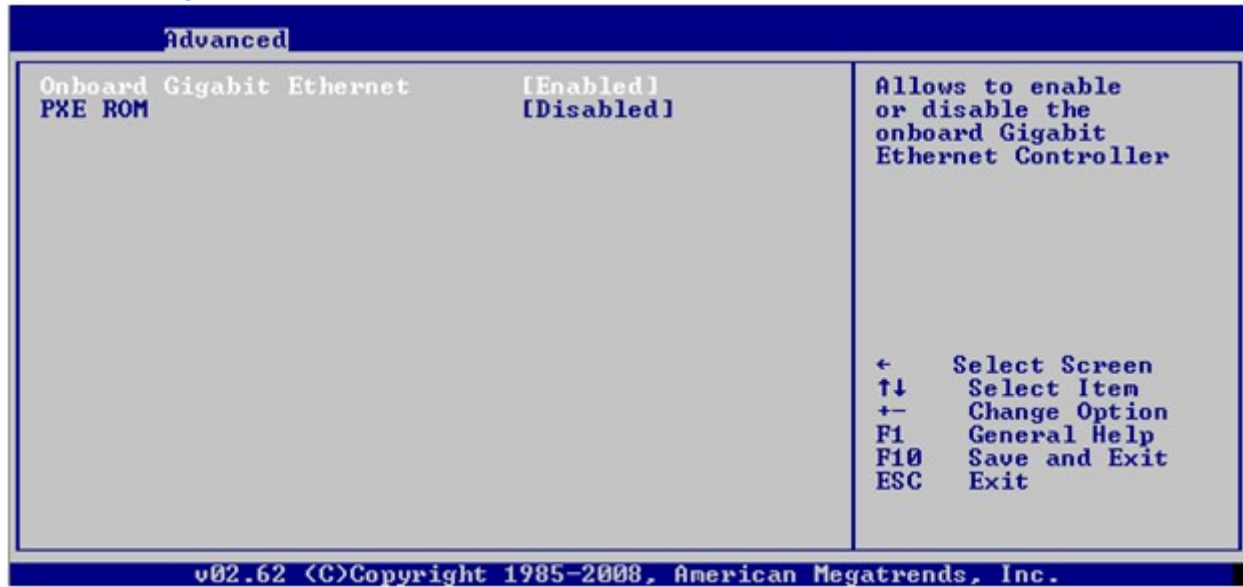
MARS Interface Configuration

Advanced		MARS Feature
MARS Interface Configuration MARS [SMB Manager] System Type : SMB Manager Power Source : AC ▶ Battery 1 ▶ Battery 2		← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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Advanced		
Battery 1 : Not Present State : N/A Manufacturer : N/A Serial Number : N/A Device Name : N/A Chemistry : N/A Current Charge : N/A Cycle Count : N/A Date Of Manufacture : N/A Charge Time : N/A Discharge Time : N/A Temperature : N/A Device Capacity : N/A Last Full Capacity : N/A		← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
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Feature	Option	Description
MARS	Disabled	Enables the MARS function
	Auto	
	SMB	
	Charger	
	SMB	
	Manager	

Ethernet Configuration



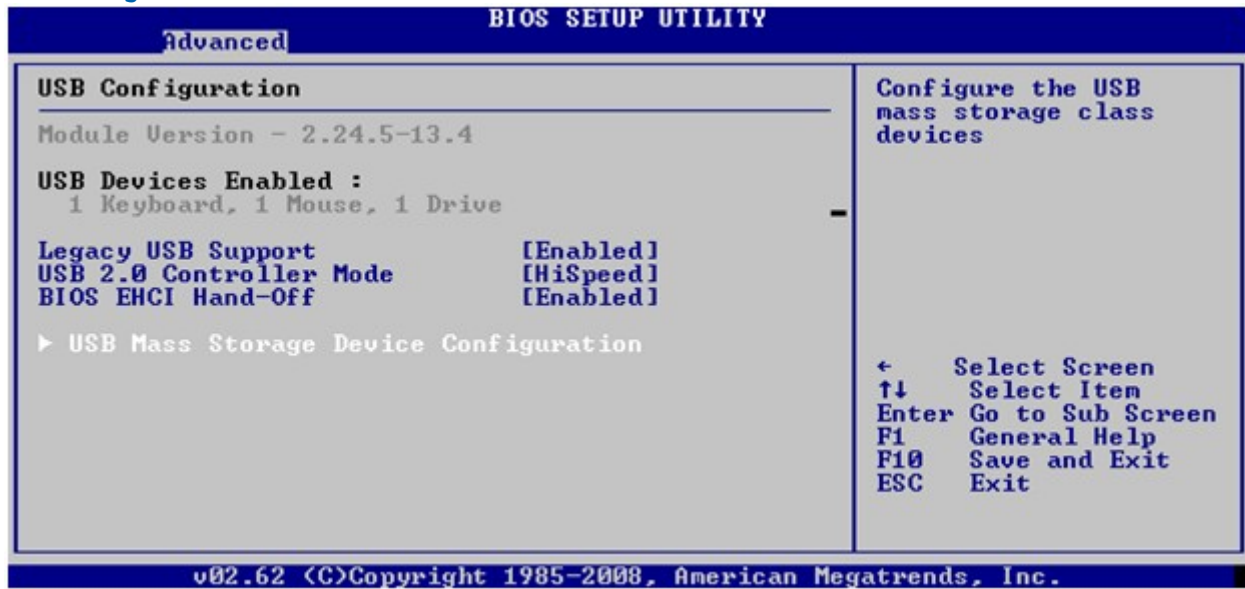
Feature	Option	Description
Onboard Gigabit Ethernet	Disabled Enabled	Disables / Enables the onboard Ethernet interface
PXE ROM	Disabled Enabled	Disables / Enables the PXE Boot ROM

PCIExpress Configuration



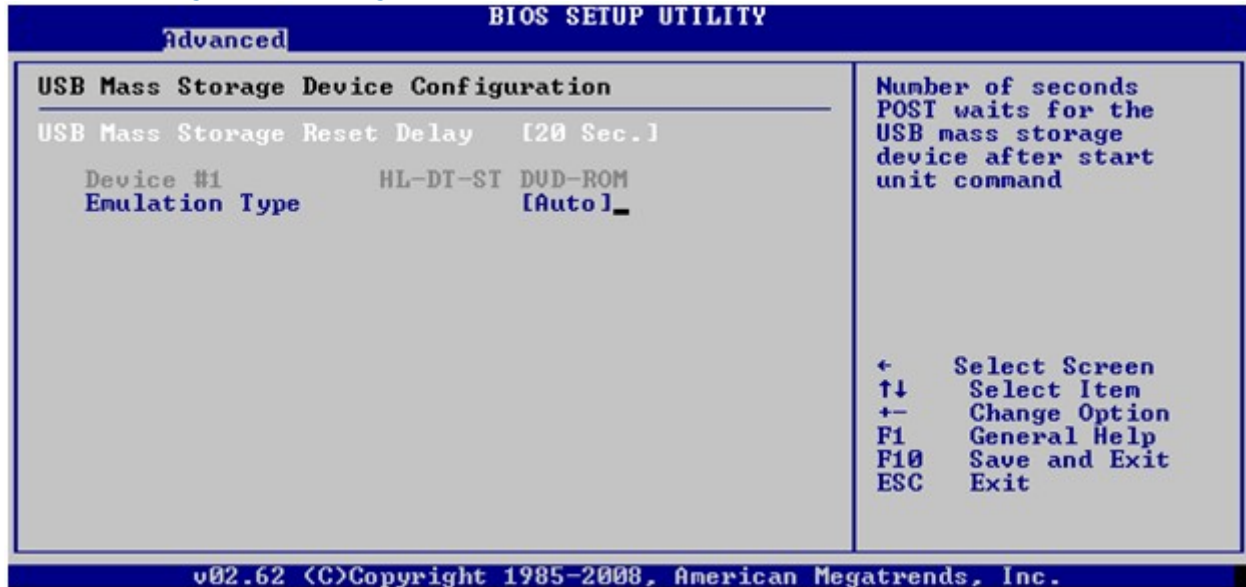
Feature	Option	Description
PCIe Ports	Both Disabled Port 0 Port 1	Disables or enables according PCI Express lanes. Onboard Gigabit Ethernet is connected to Port 1. Port 0/1: enables specific PCI Express Lane Both: Both PCI Express lanes from US15W SCH are enabled Disabled: US15W SCH PCI Express is completely disabled
PCIE Base Spec Compliance	Disabled Enabled	Allows to choose between strict PCIE base specification compliance and power saving mode. Warning: Disabling PCIE compliance might influence the PCIE lane throughput.
SDVO PCIE Base Spec Compliance	Disabled Enabled	Allows to choose between strict PCIE base specification compliance and power saving mode. Warning: Disabling SDVO compliance might influence the PCIE lane throughput.
Active State Power Management	Disabled Enabled	Enables/Disables PCI Express L0 and L1 link power states.

USB Configuration



Feature	Option	Description
Legacy USB Support	Disabled Enabled	Enables / disables support for legacy USB.
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled Enabled	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver

USB Mass Storage Device Configuration



Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto USB devices with less than 20MB will be emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Hardware Health Configuration

Advanced Hardware Health Monitoring

Module Hardware Health Configuration

H/W Health Function [Enabled]

CPU Temperature : 46°C/114°F
 Module Temperature : 29°C/84°F
 Chipset Sensor #1 : < 51°C/123°F
 Chipset Sensor #2 : < 51°C/123°F

Baseboard Hardware Health Configuration

H/W Health Function [Enabled]

Temperature Sensor #1 : 124°C/255°F
 Temperature Sensor #2 : 124°C/255°F
 Temperature Sensor #3 : 124°C/255°F

Fan1 Speed Selector : [4]
 Fan1 Ticks per Rev : [2]
 Fan1 Speed : 3879 RPM
 Fan2 Speed Selector : [4]
 Fan2 Ticks per Rev : [2]
 Fan2 Speed : No Function
 Fan3 Speed Selector : [4]
 Fan3 Ticks per Rev : [2]
 Fan3 Speed : No Function

UcoreA : 3.645 U
 UcoreB : 3.612 U
 +3.3Vin : 3.387 U
 +5Vin : 5.053 U
 +12Vin : 12.281 U
 -12Vin : -14.697 U
 -5Vin : -5.954 U
 +5USB : 5.043 U
 VBAT : 3.403 U

Enables Hardware Health Monitoring Device.

← Select Screen
 ↑↓ Select Item
 +- Change Option
 F1 General Help
 F10 Save and Exit
 ESC Exit

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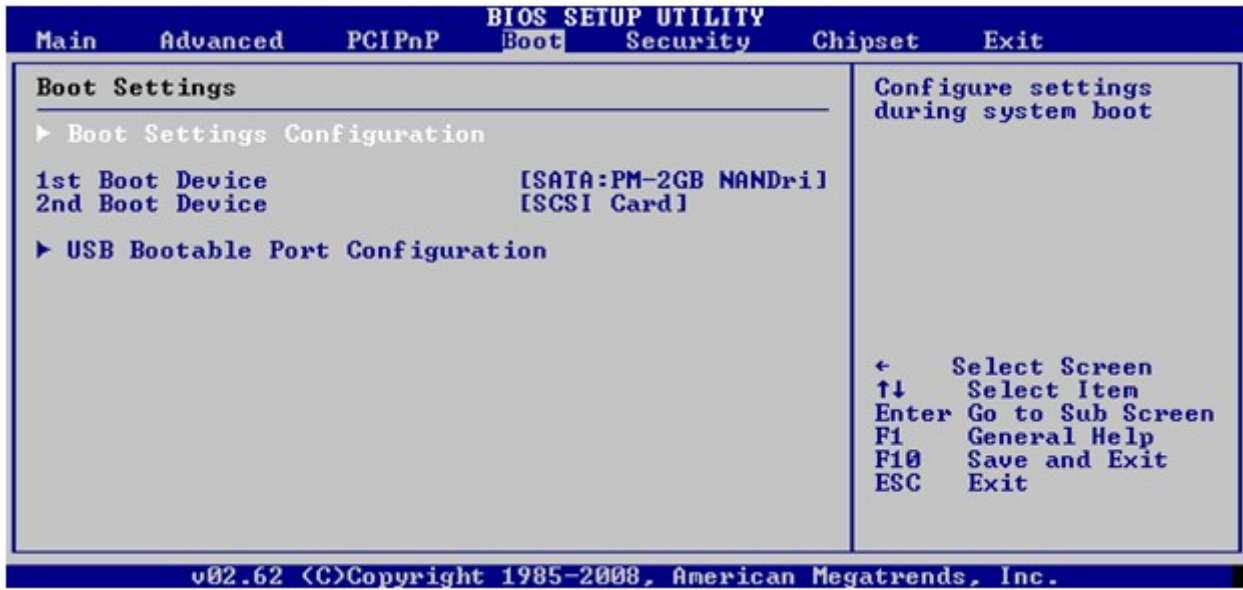
Feature	Option	Description
Module HWM: H/W Health Function	Disabled Enabled	Enables the onboard Hardware Health Monitoring Device CPU Temperature: CPU ACPI temperature Module Temperature: Internal temperature of HWM Chipset Sensor #1 / Chipset Sensor #2: Internal thermal sensors of US15W SCH to cause main memory throttling and display refresh throttling. See JIDA32/K-Station resource list for more details
Baseboard HWM: H/W Health Function	Disabled Enabled	Enables the Hardware Health Monitoring support for external LPC I/O Winbond 83627
Fan Speed Selector	1 2 4 ... 128	Select the FAN Speed Divisor according to nominal revolutions per minute of used FAN: Divisor 1: 8800 rpm, Divisor 2: 4400 rpm Divisor 4: 2200 rpm, Divisor 8: 1100 rpm Divisor 16: 550 rpm, Divisor 32: 275 rpm Divisor 64: 137 rpm, Divisor 128: 68 rpm
Fan Ticks per Rev	1 2 4 8	Number of Ticks per Revolution

7.3.4 Advanced PCI/PnP Settings

Main		Advanced	PCI/PnP	Boot	Security	Chipset	Exit
Advanced PCI/PnP Settings							Clear NURAM during system boot
WARNING: Setting wrong values in below sections may cause system to malfunction.							
Clear NURAM				[No]			
PCI Latency Timer				[64]			
PCI IDE BusMaster				[Enabled]			
IRQ3				[Available]			
IRQ4				[Available]			
IRQ5				[Available]			
IRQ6				[Available]			← Select Screen
IRQ7				[Available]			↑↓ Select Item
IRQ9				[Available]			+− Change Option
IRQ10				[Available]			F1 General Help
IRQ11				[Available]			F10 Save and Exit
IRQ15				[Available]			ESC Exit
Reserved Memory Size				[Disabled]			
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Feature	Option	Description
Clear NVRAM	No Yes	Clear NVRAM once during next system boot.
PCI Latency Timer	32 64 ... 248	Value in units of PCI clocks for PCI device latency register
PCI IDE BusMaster	Disabled Enabled	Disables and enables PCI IDE Busmaster
IRQ3 ... IRQ15	Available Reserved	Available: IRQ useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices
Reserved Memory Size	Disabled 16k 32k 64k	Size of memory block to reserve for legacy ISA devices

7.3.5 Boot

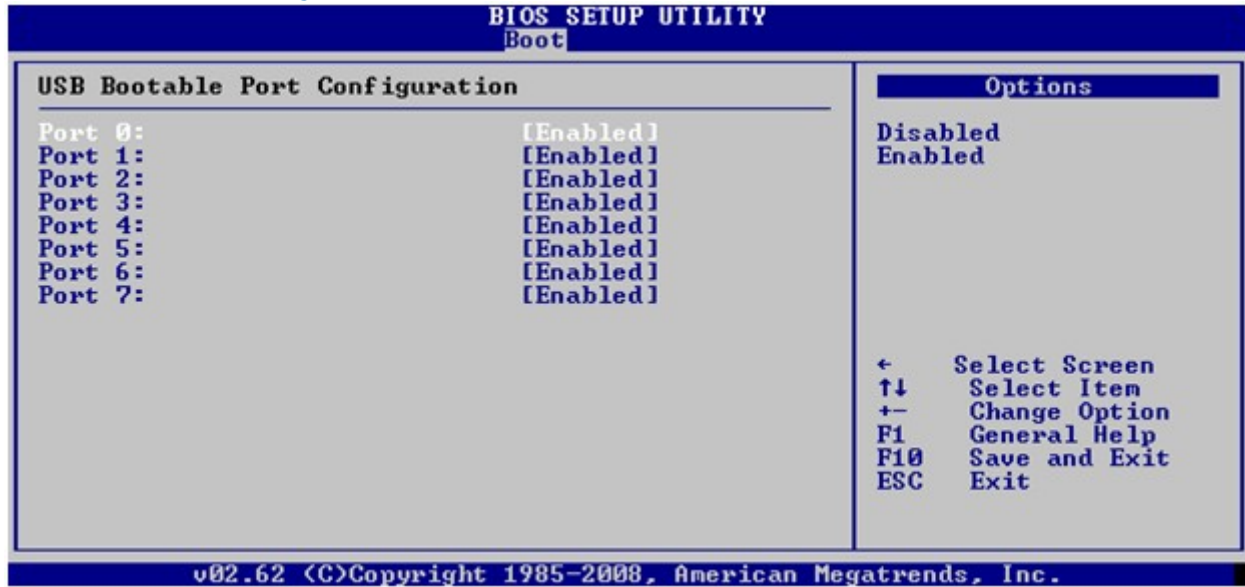


Boot Setting Configuration



Feature	Option	Description
Dark Boot	Disabled Enabled	Disabled: Shows normal POST messages Enabled: Shows OEM Logo during boot up
AddOn ROM Display Mode	Force BIOS Keep Current	Set Display Mode for Option ROM
Bootup Num-Lock	On Off	Select Power-On state for Num-Lock
PS/2 Mouse Support	Auto Disabled Enabled	Disables and enables or auto selects PS/2 Mouse Support
Wait For 'F1' If Error	Disabled Enabled	Wait for F1 key to be pressed, if error
„Press DEL“ Message Display	Enabled Disabled	Enabled allows the BIOS to display the message Press DEL to run Setup after memory initialization. Disabled suppresses this message
Boot USB HDD first	Disabled Enabled	If enabled, boots new attached USB HDD always first. If disabled, sets new attached USB HDD to last boot position
Interrupt 19 Capture	Disabled Enabled	Allows option ROMs to trap INT19h if enabled

USB Bootable Port Configuration



Feature	Option	Description
Port 0 - 7	Disabled Enabled	Enables/Disables a specific port to be bootable

7.3.6 Security



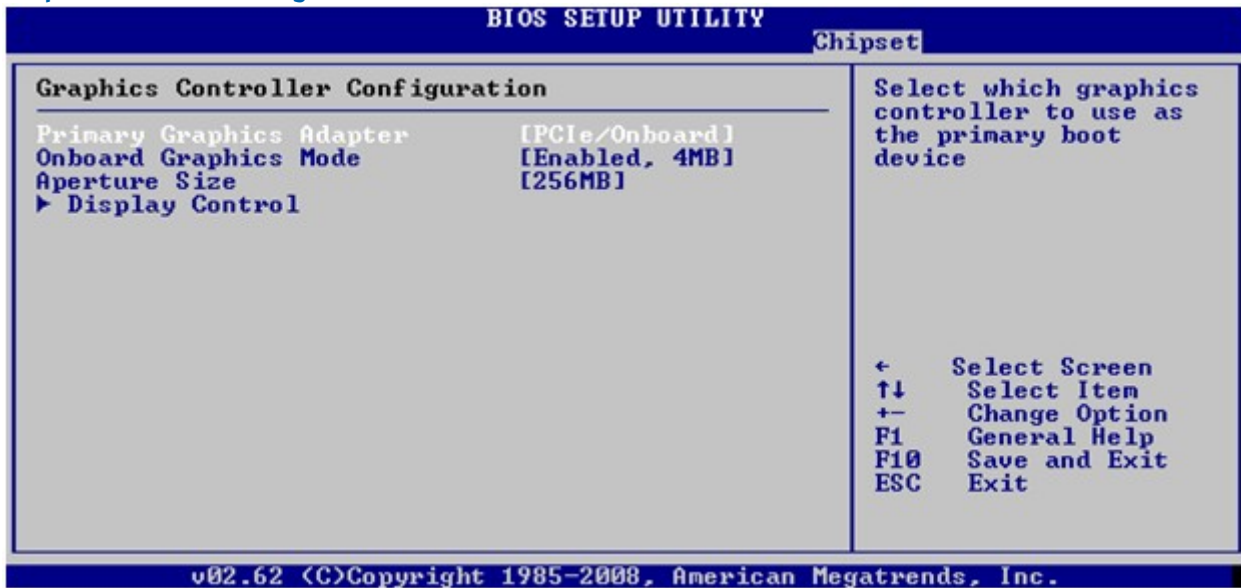
Feature	Option	Description
Change Supervisor Password	Type in	
Change User Password	Type in	
Boot Sector Virus Protection	Disabled Enabled	Enables or disables boot sector virus protection.

7.3.7

7.3.8 Advanced Chipset Settings



Graphic Controller Configuration



Feature	Option	Description
Primary Graphic Adapter	PCIe/Onboard Onboard	Selects which graphics controller is used as primary boot device (boot sequence)
Onboard Graphic Mode	Disabled Enabled, 1MB Enabled, 4MB Enabled, 8MB	Selects the amount of pre-allocated system memory used by the onboard graphics controller
Aperture Size	256MB 128MB	Configures the size of the aperture space. Needs IEGD driver.

Display Control



Feature	Option	Description
Boot Display Device	Auto LVDS SDVO- CRT SDVO- DVI/HD MI	Select the Boot Display Device. Note: SDVO is not supported on HW Rev CE 1.x.x (PCB L130)

Internal LVDS Configuration

Current LVDS Configuration		Options
Data Source	: LVDS - DVI ID	Auto
Resolution	: 1024x768	Fixed Mode
Color Depth	: 24Bit	PAID
Channel Count	: Single Channel	FPID
Dithering	: Disabled	
Flat Panel Mode	[Auto]	
Auto Fallback	[Fixed Mode]	
Flat Panel Type	[SVGA 800x600]	
PAID/FPID	[3]	
Color Depth	[18Bit]	
Local Flat Panel Scaling	[Stretched]	
LVDS -> DVI ID	[?]	
Backlight Control Type	[I2C]	
Backlight Brightness	[128]	
		← Select Screen
		↑↓ Select Item
		+− Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit

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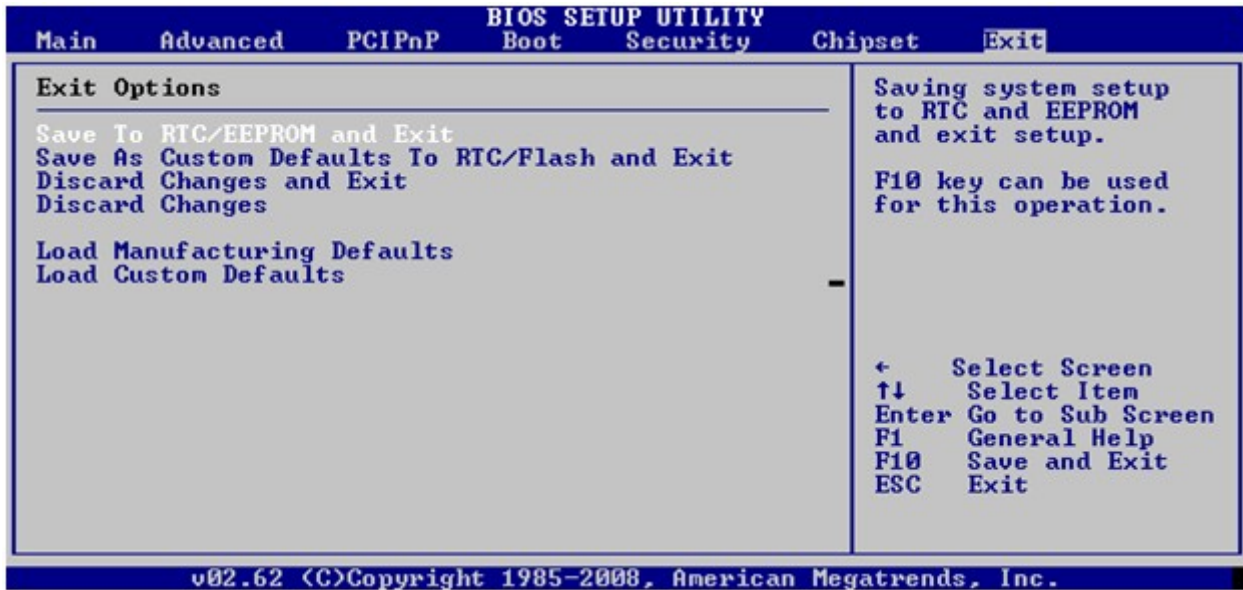
Feature	Option	Description
Flat Panel Mode	Auto Fixed Mode PAID FPID	Selects the Mode for the flat panel detection
Auto Fallback	Disabled Fixed Mode	Selects what happens, when there is no EEPROM detected (only when FPM: Auto)
Flat Panel Type	VGA 640x480 SVGA 800x600 ... WXGA 1280x800	Selects the resolution of the LVDS display (only in FMP: Fixed Mode)
PAID/FPID	[X]	Selects the number of the PAID/FPID
Color Depth	18bit 24bit	Selects the Color Depth of the connected LVDS display (only in FPM: Fixed Mode)
Local Flat Panel Scaling	Centered Stretched Disabled	Selects the Scaling Options for the LVDS panel (only in FPM: Fixed Mode)
LVDS → DVI ID	5 7	Select the type of used LVDS to DVI converter 5 = 1x18bit Adapter, 7 = 1x24bit Adapter
Backlight Control Type	None/External I2C PWM	Selects the mode for Backlight Control
Backlight Brightness	[0...255]	Selects the default setting for Backlight Brightness

System Controller Hub Configuration



Feature	Option	Description
USB UHCI Controller	Disabled 2 USB Ports 4 USB Ports ... 8 USB Ports	Enables / Disables USB ports
USB EHCI Controller	Enabled Disabled	Controls EHCI (USB 2.0) functionality for all the UHCI ports set to active state
USB Client Controller	Enabled Disabled	This enables the USB client functionality on COM Express USB Port #7
Audio Controller	HDAudio Disabled	Enables / Disables the HDA audio controller
Serial IRQ Mode	Continuous Quiet	Defines the serial IRQ mode (Quiet = the chipset communicates only if an IRQ is triggered) for the LPC interface

7.3.9 Exit Menu



Feature	Description
Save To RTC/EEPROM and Exit	Saving system setup to RTC and EEPROM and exit setup. F10 key can be used for this operation
Save As Custom Defaults To RTC/Flash and Exit	Saving system setup as custom defaults to RTC and Flash and exit setup. F11 key can be used for this operation. Refer to Flash Backup Feature for more details
Discard Changes and Exit	Exit system setup without saving any changes. ESC key can be used for this operation
Discard Changes	Discards changes done so far to any of the setup questions. F7 key can be used for this operation
Load Manufacturing Defaults	Load manufacturing default values for all the setup questions. F9 key can be used for this operation
Load Custom Defaults	Load custom default values for all the setup questions.

8 Document Revision History

Revision	Date	Edited by	Changes
NOW1M101	17.07.08	HAM	Initial Release
NOW1M102	10.10.08	HAM	Several modifications
NOW1M110	03.12.08	HAM	Added heat spreader mounting, LPC and SMBus addresses
NOW1M111	19.01.09	HAM	Added SDIO information, updated BIOS settings ...
NOW1M120	20.01.09	UMA	Small changes, added power measurements, added warning for LPC clock zero delay buffer, simplified chapter 18. (power supply)
NOW1M130	20.05.09	PRO	Changed Layout to new Kontron Design, Updated Module specifications, Updated Block Diagram, Added current available module types and specifications of used onboard SSD Flash, Updated Power Consumption, Added MTBF, Updated detailed Graphics Memory Information, Corrected GPIO description, Added Technology Information Chapter, Added Setup Screenshots and updated description to BIOS NOW1R112
NOW1M131	17.07.09	PRO	Updated Design to final CI, Updated Layout and content to KEM standard for modules, Corrected BIOS Resource List, Added USB to Wake Up Events from S3, Added Heat spreader and Heatsink Descriptions, Updated SDIO Description, Corrected GPIO description and added speed limitation, Updated Electrical Specification with general Power Supply Rise time for modules, Updated PCI Express description, Added J1400 onboard connector description, Added Note for SATA, Added Flash Backup Feature description, Added I2C bus speed tables, Updated Pin-out List to hardware revision CE 1.7.0 and added terminations, Updated BIOS chapter to BIOS revision NOW1R113
NOW1M132	31.07.09	PRO	Corrected USB Port numbering for USB 6/7
NOW1M133	02.11.09	PRO	Updated resource list and removed LPC resources, Corrected Power Control description, Removed Heat spreader. Documentation is only available in EMD Customer Section, Added K-Station / JIDA32 resource list, Updated BIOS chapter to BIOS revision NOW1R114
NOW1M134	06.11.09	PRO	Removed wrong information for upcoming hardware revision CE 4.x.x
NOW1M140	24.02.10	PRO	Updated manual to redesign revision CE 4.5.0, Updated BIOS chapter to BIOS revision NOW1R116
NOW1M141	09.09.10	UMA	Switched to new documentation system, removed appendices, updated BIOS chapter to BIOS revision NOW1R117

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