

# FrameLocker



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## Monochrome Video Frame Grabber PC/104 Card

### Technical Reference Manual

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**Rev 2.0** Jan 18, 1999



# NOTICE

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## B. CAUTION!

- 1 ALWAYS CHECK voltage levels before connecting any **FrameLocker** interface pin to any device or voltage source. DO NOT INTERCONNECT any **FrameLocker** interface pins before checking voltage levels and pinouts on connectors.
- 2 DO NOT SHORT or ground any output.
- 3 AVOID STATIC ELECTRICITY. The products herein contains devices that might be damaged by static electricity.

SERIOUS DAMAGE may result to **FrameLocker** and/or the computer and WARRANTY will be VOID if these rules are not followed.

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Thank you for purchasing the **FrameLocker** Monochrome Video Frame Grabber board. We believe the quality, reliability and overall performance of this product will help you achieve a completely satisfactory image processing system.

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In case you would need technical assistance, although we do not anticipate you will encounter any problems using the ANDI products, please document the situation thoroughly and contact Ajeco by telefax or letter. We also greatly appreciate if you have specific ideas, which might help us improve our products. Please send us your ideas in writing.

Finally, We wish to thank you once again for your excellent choice of ANDI products.

Sincerely Yours,

AJECO INC (OY)

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Place of purchase: \_\_\_\_\_

**FrameLocker** card number: \_\_\_\_\_

Notes: \_\_\_\_\_

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## FrameLocker Video Digitizer Board

This document is a general description of the FrameLocker video frame grabber board. In order to keep this document small and compact, we do not include the specifications of the Bt819 video front end chip here within. The Bt819 specifications can be downloaded from Ajeco's web site [www.ajeco.com](http://www.ajeco.com)

FrameLocker is a monochrome, 2 video input PC/104 video capturing board, designed to provide easy and low cost access to standard video signals. The board captures video images and stores them in its internal buffer memory: The captured images can be uploaded from the boards memory to a host CPU for further (image) processing.

FrameLocker is suitable for image capturing and processing, remote surveillance, machine vision and virtually any application where black and white video image capturing is desired. The board features a video front end chip that allows for adjusting of image brightness, contrast and resolution in addition to numerous other adjustments that optimize the image capturing task. Please refer to the Bt819 register specifications for a closer description on FrameLocker's capabilities.

### 1. The Base Address Settings

BS2	BS1	BS0	Base Address (Hex)
C	C	C	0x0
C	C	O	0x80
C	O	C	0x100
C	O	O	0x180
O	C	C	0x200
O	C	O	0x280
<b>O</b>	<b>O</b>	<b>C</b>	<b>0x300 default</b>
O	O	O	0x380

**Table 1. Base addresses on the FrameLocker**

There are 3 jumpers, BS2, BS1, and BS0. The board is shipped set to base address 0x300. In the above table the letter 'C' stands for closed and letter 'O' for open.

## 2. The Interrupt Line Selection Jumpers

The board will always generate an interrupt when an image digitization has been finished. However, it is not necessary to use the IRQ, the demo programs run without interrupts, so please leave the jumper open. The possible interrupt lines are IRQ2 to IRQ7, as marked on the boards silk screen printing.

DMA is not supported on FrameLocker.

## 3. The Video Front End Bt819

Almost all functionality of the board is contained inside the Bt819 video digitizer chip. Please, refer to the Bt819 documents for a register description on the chip. We strongly recommend downloading the Bt819 specifications from Ajeco's web-site or contact Ajeco to obtain a copy of the specs. The Bt819 chip is accessed through the library functions in the FLLIB.C module, that rely on the FL\_send\_i2c() and FL\_read\_i2c() library functions. Please refer to the FL.C demo program for the usage of the library functions.

## 4. I/O Port Descriptions

The board does not use any extended or expanded memory in the PC architecture. Being totally I/O decoded, it is easily used from operating systems running in protected mode, without need for writing special device driver programs. Contact Ajeco for further information on software drivers.

The FrameLocker is totally I/O decoded and it uses the following addresses:

- Base + 0 - I2C communication**
- Base + 1 - Reserved**
- Base + 2 - Pixel Data from the board (like a FIFO)**
- Base + 3 - Control register**
- Base + 4 - Trigger control register**
- Base + 5 - Hardware reset register**

## 5. Control Register Bit Explanations

### 5.1 Image capturing

When writing to Base + 3, the bits 0 and 1 have the following meanings: Setting bit0 from '0' to '1', while bit1 is '1', starts digitization of the first field in the video frame. This result in 313 or 262 converted scanlines depending on whether the video signal is of PAL or NTSC type. This option is called Fast Conversion Mode, abbreviated as FCM.

Setting bit0 from '0' to '1' while bit1 is '0', digitizes the full video frame ((625/525 scanlines) PAL/NTSC). Note that the video front-end chip Bt819 can also be programmed for different resolution requirements. See Bt819 documentation for further information.

### 5.2 Image uploading

The bit0 of the control register (Base + 3) can be monitored for determining when the image has been completely digitized. The bit0 falls from '1' to '0' indicating a digitized image. A short delay must then be introduced before attempting to upload the image. This allows the board to settle before the image is read. A convenient way to produce a short delay is to read an unused I/O port as shown in the demo/test program FL.C (FLLIB.C).

Writing a '0' to the control register's bit0 sets the board in an uploading mode, and pixels can be read as a continuous stream from the data register Base + 2. Note, that the video front-ends HACTIVE register determines the number of pixels per scanline. Refer to the Bt819 register description and the FL.C demo/test source code for further information.

## 6. Demo/Test Program

The test code supplied with the card allows you to grab a frame and display it on a VGA screen. It assumes base 300h. Start the code with the instruction:

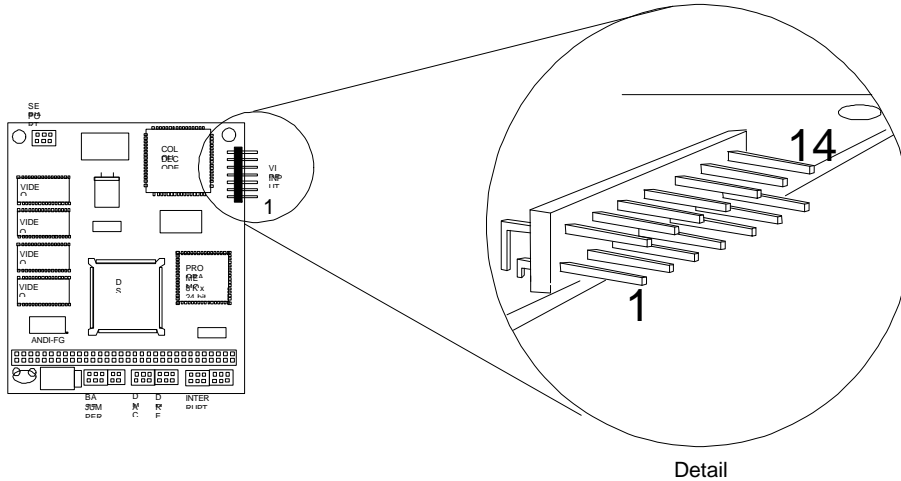
**FL -n < or > FL -p**

Where -n stands for NTSC and -p for PAL. The test program assumes that you connect a video source to channel 1 (not to channel 0). This way you know that the communication to the video front end chip (bt819) is OK, because the test does not use the default input. Connect your video source to pin9 of the input connector P1 on the board.

The demo program sets the video display to the standard VGA 320x200 mode with 256 gray shades. The image on the display shows both the odd and even fields of the video. The demo program has a simple menu that allow adjusting of brightness, contrast, number of lines and pixels in the image etc. Refer to the FL.C for a more detailed description on the menu.

## 7. Input Connector P1

The input connector P1 has the following pinout:



Pin Number	Function
1	Reserved, do not use
2, 4, 6, 8, 10,12, 13, 14	Ground
7	Video Input Channel 0
9	Video Input Channel 1
3, 5, 11	Reserved, do not use

### Note !

Observe that the boards inputs are protected by clamping diodes. All voltages above VCC +0.5 volts are clamped (conducted to) to VCC. All voltages below GND -0.5 volts are clamped (shorted to) to GND.

The video level should be 1Vpp. The board features an automatic gain control (AGC), that can be turned on or off from software.

\* end of document \*