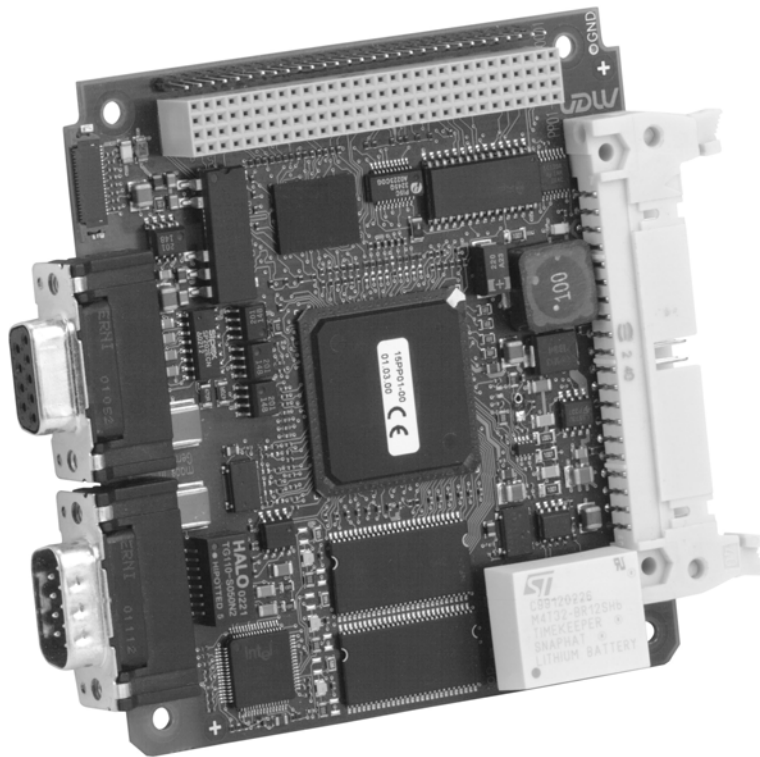


# PP1 – PCI-104 Module with MPC5200/B



User Manual

## PP1 – PCI-104 Module with MPC5200/B

The PP1 is controlled by an MPC5200/B PowerPC® that operates at 384 MHz. The complete PCI-104 module is exclusively available for -40 to +85°C operation temperature, as is the MPC5200 itself. The CPU consumes less than 1 W at 384 MHz.

The PP1 provides up to 128 MB SDRAM for data and 16 MB Flash memory for program storage as well as 64 KB FRAM. The bus interface is a 32-bit 33-MHz PCI bus. The PP1 provides two optically isolated RS232 and one Fast Ethernet interface at its front panel. Two CAN controllers are included in the MPC5200. The physical CAN interface can be located on SA-Adapters™ or on the carrier board. The board also features a real-time clock and watchdog.

The PP1 comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

The PP1 is an industrial computer which is designed to operate under harsh environmental conditions. It complies with the PCI-104 specification and can be stacked with other PCI-104 boards or mounted on different types of carrier boards.

## Technical Data

### **CPU**

---

- PowerPC®
  - MPC5200 or MPC5200B
  - 384MHz

### **Memory**

---

- Up to 128MB SDRAM system memory
  - Soldered
  - 64MHz memory bus frequency
- 16MB Flash
- 64KB non-volatile FRAM
- Serial EEPROM 16kbits for factory settings

### **I/O**

---

- Ethernet
  - 10/100Base-T Ethernet
  - 9-pin D-Sub connector at front panel

- Two RS232 UARTs (COM1/COM2)
  - One 9-pin D-Sub connector at front panel
  - Data rates up to 115.2kbits/s
  - 512-byte transmit/receive buffer
  - Handshake lines: none
- USB
  - One USB 1.1 port
  - Physical line interface via SA-Adapter™ on I/O connector P2
  - OHCI implementation
  - Data rates up to 12Mbits/s
- Two independent CAN interfaces
  - Physical line interface via SA-Adapters™ on I/O connector P2
- Display interface
  - Four characters, 5 by 7 pixels
  - For additional display adapter PCB (on request)
- 8 GPIO lines
  - Accessible via I/O connector P2

---

#### **Front Connections**

- One Ethernet (D-Sub)
- Two RS232 UARTs COM1/COM2 (D-Sub)

---

#### **PCI Interface**

- 32-bit/33-MHz PCI interface at PCI-104 connector J1
- V(I/O): +3.3V (not +5V tolerant)
- Compliant with PCI Specification 2.2
- Support of one external master

---

#### **Miscellaneous**

- Real-time clock
- Temperature sensor
- Three push buttons and LED on optional display PCB (on request)

---

#### **Electrical Specifications**

- Supply voltage/power consumption:
  - +5V, ±5%, 100mA typ.
  - +3.3V, ±5%, 900mA typ.
- MTBF: 450,000h @ 40°C (derived from MIL-HDBK-217F)

---

#### **Mechanical Specifications**

- Dimensions: conforming to PCI-104 specification
- Weight: 90g

---

### **Environmental Specifications**

---

- Temperature range (operation):
  - -40..+85°C
  - Airflow: min. 10m<sup>3</sup>/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

### **Safety**

---

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

### **EMC**

---

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst) with regard to CE conformity


### **BIOS**

---

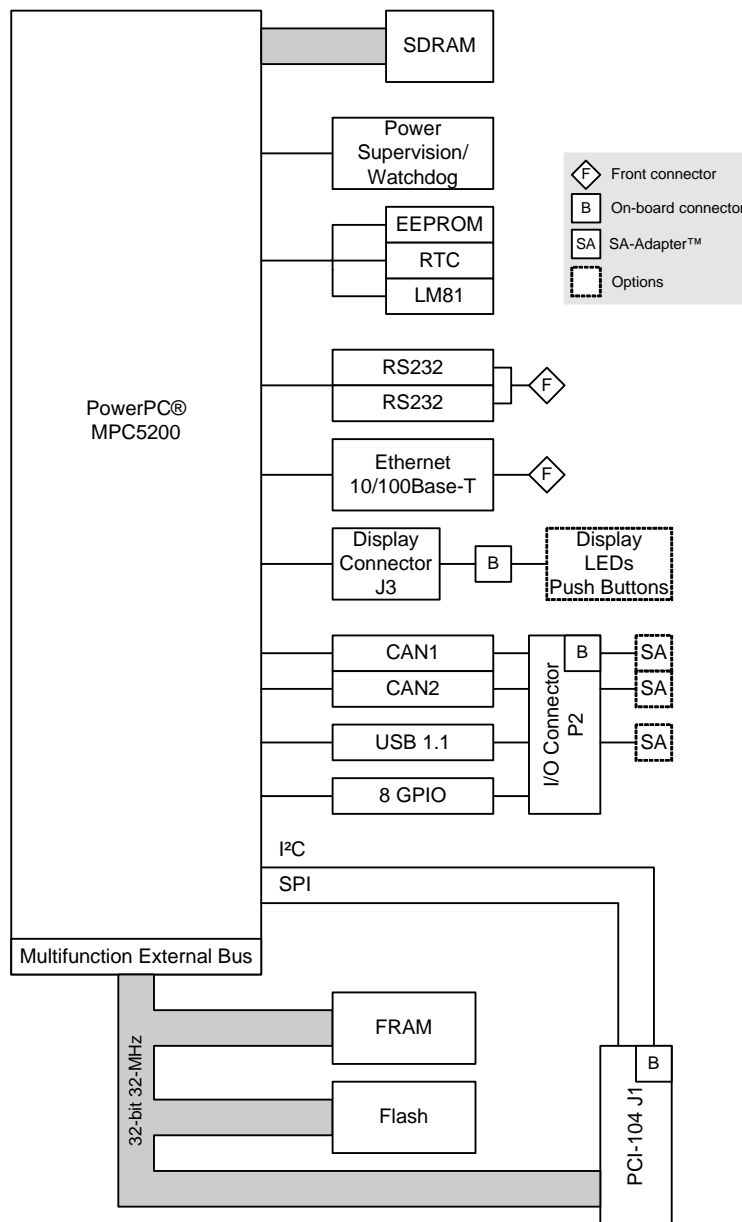
- MENMON™

### **Software Support**

---

- VxWorks®
- Linux
- CANopen firmware (Vector Informatik)
- CANopen support: MEN Driver Interface System (MDIS™ for Windows®, Linux, VxWorks®, QNX®, RTX, OS-9®)
- MSCAN/Layer2 support: MEN Driver Interface System (MDIS™ for Windows®, Linux, VxWorks®, QNX®, RTX, OS-9®)
-  For more information on supported operating system versions and drivers see [online data sheet](#).

# Block Diagram



## Configuration Options

### ***CPU***

---

- MPC5200 or MPC5200B, 384 MHz

### ***Memory***

---

- System RAM
  - 32 MB, 64 MB or 128 MB
- Flash
  - 2 MB, 4 MB, 8 MB or 16 MB
- FRAM
  - 0 KB, 32 KB or 64 KB

**Please note that some of these options may only be available for large volumes.  
Please ask our sales staff for more information.**

## Product Safety



### Lithium Battery

**This board contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced!**

Replace only with the same or equivalent type.

Dispose of used batteries according to the manufacturer's instructions.

See [Chapter 5 Maintenance on page 47](#).



### Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

## About this Document

This user manual describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

### History

Edition	Comments	Technical Content	Date of Issue
E1	First edition	H. Schubert, U. Franke	2004-05-14
E2	General update; new MENMON version	H. Schubert, U. Franke	2008-04-10

### Conventions



This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

*italics*

Folder and file names are printed in *italics*.

**bold**

**Bold** type is used for emphasis.

hyperlink

Hyperlinks are printed in blue color.



The globe will show you where [hyperlinks](#) lead directly to the Internet, so you can look for the latest information online.

0xFF

Hexadecimal numbers are preceded by "0x", which is the usual C-language convention, and are printed in a monospace type, e.g. 0x00FFFF.

IRQ#  
/IRQ

Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out

Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".



Vertical lines on the outer margin signal technical changes to the previous edition of the document.

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# Contents

<b>1</b>	<b>Getting Started</b>	<b>14</b>
1.1	Map of the Board	14
1.2	Installation Check List	15
1.3	Installing Operating System Software	15
<b>2</b>	<b>Functional Description</b>	<b>16</b>
2.1	Power Supply	16
2.1.1	Reset Control and Watchdog	16
2.2	Temperature Sensor	18
2.3	Clock Supply	18
2.4	Real-Time Clock	18
2.5	PowerPC CPU	18
2.6	Memory	19
2.6.1	SDRAM	19
2.6.2	Flash	19
2.6.3	FRAM	19
2.6.4	EEPROM	19
2.7	Serial Ports COM1/COM2	20
2.7.1	Fuse Protection	21
2.8	Ethernet	22
2.8.1	Implementation on PP1	22
2.8.2	General	23
2.8.3	10Base-T	23
2.8.4	100Base-T	23
2.9	I/O Connector – CAN Bus, USB, GPIO, Reset	24
2.9.1	CAN Bus	26
2.9.2	USB	26
2.9.3	GPIO	26
2.9.4	Fuse Protection	26
2.10	Alphanumeric Display	27
2.10.1	Fuse Protection	28
2.11	PCI-104 Interface J1	29
<b>3</b>	<b>MENMON</b>	<b>31</b>
3.1	General	31
3.1.1	State Diagram	32
3.2	Interacting with MENMON	34
3.2.1	Entering the Setup Menu/Command Line	34
3.3	Configuring MENMON for Automatic Boot	34
3.4	Updating Boot Flash	35
3.4.1	Update via the Serial Console using SERDL	35
3.4.2	Update from Network using NDL	35
3.5	Diagnostic Tests	36

3.6	MENMON Configuration and Organization	37
3.6.1	Consoles	37
3.6.2	MENMON Memory Map	38
3.6.3	MENMON BIOS Logical Units	39
3.6.4	System Parameters	40
3.7	MENMON Commands	43
<b>4</b>	<b>Organization of the Board</b>	<b>45</b>
4.1	Memory Mappings	45
4.2	Interrupt Handling	46
4.3	SMB Devices	46
<b>5</b>	<b>Maintenance</b>	<b>47</b>
5.1	Lithium Battery	47
<b>6</b>	<b>Appendix</b>	<b>48</b>
6.1	Literature and Web Resources	48
6.1.1	PCI-104	48
6.1.2	PowerPC Processor	48
6.1.3	Ethernet	48
6.1.4	USB	48
6.1.5	Hardware Monitor	48
6.2	Finding out the Board's Article Number, Revision and Serial Number	49

---

## Figures

Figure 1. Map of the board – top view. . . . .	14
Figure 2. Position of watchdog configuration resistor RC1 on top side of the board . . . . .	17
Figure 3. Position of fuse for COM protection on top side of the board . . . . .	21
Figure 4. Position of fuse for CAN bus and USB protection on top side of the board . . . . .	26
Figure 5. Position of fuse for display protection on top side of the board. . . . .	28
Figure 6. MENMON – State Diagram, Degraded Mode/Full Mode . . . . .	32
Figure 7. MENMON – State Diagram, Main State . . . . .	33
Figure 8. Interrupt Handling . . . . .	46
Figure 9. Position of Lithium Battery on PP1 . . . . .	47
Figure 10. Labels giving the board’s article number, revision and serial number. . . . .	49

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## Tables

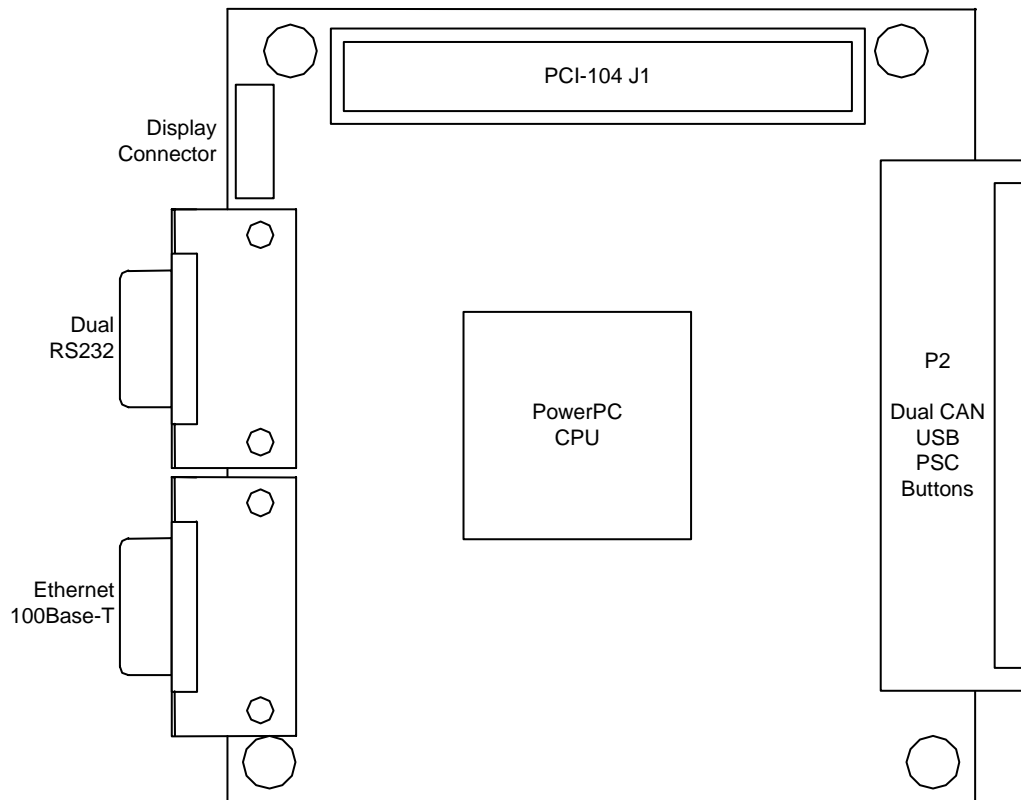
Table 1.	Pin assignment of 9-pin D-Sub COM1/COM2 connector . . . . .	20
Table 2.	Signal mnemonics for serial COM 1/2 port . . . . .	20
Table 3.	Pin assignment of the 9-pin D-Sub Ethernet connector . . . . .	22
Table 4.	Signal mnemonics for Ethernet 100Base-TX interface . . . . .	22
Table 5.	Pin assignment of the 40-pin I/O connector P2 . . . . .	24
Table 6.	Signal mnemonics of 40-pin I/O connector P2 . . . . .	25
Table 7.	Pin assignment of the 20-pin display connector. . . . .	27
Table 8.	Signal mnemonics for display interface . . . . .	27
Table 9.	Mnemonics of special signals of PCI J1. . . . .	29
Table 10.	Pin assignment of PCI J1 . . . . .	30
Table 11.	MENMON – Program Update Files and Locations . . . . .	35
Table 12.	MENMON – Diagnostic tests. . . . .	36
Table 13.	MENMON – System Parameters for Console Selection . . . . .	37
Table 14.	MENMON – Address Map (Full-featured mode) . . . . .	38
Table 15.	MENMON – Boot Flash Memory Map (16 MB). . . . .	38
Table 16.	MENMON – Controller Logical Units (CLUNs). . . . .	39
Table 17.	MENMON – Device Logical Units (DLUNs) . . . . .	39
Table 18.	MENMON – PP1 system parameters. . . . .	40
Table 19.	MENMON – Reset Causes through System Parameter rststat. . . . .	42
Table 20.	MENMON – Command Reference . . . . .	43
Table 21.	Memory Map – Processor View. . . . .	45
Table 22.	Memory Map – PCI View . . . . .	45
Table 23.	BATS set up by MENMON . . . . .	45
Table 24.	SMB Devices . . . . .	46

# 1 Getting Started

This chapter will give an overview of the board and some hints for first installation in a system.

## 1.1 Map of the Board

**Figure 1.** Map of the board – top view



## 1.2 Installation Check List

You can use the following "check list" to install the module for the first time and to test proper functioning of the board.

- Power-down the system.
- Install the PCI-104 module in your system, e.g. on another PCI-104 module.
- Connect a terminal to the RS232 D-Sub connector. Note that the connector has no standard RS232 pinout. It incorporates two RS232 interfaces. See [Chapter 2.7 Serial Ports COM1/COM2 on page 20](#) for the pin assignment. MEN offers an adapter for easy connection of standard RS232 cables. See MEN's [website](#) for ordering information.
- Set your terminal to the following protocol:
  - 115,200 baud data transmission rate
  - 8 data bits
  - 1 stop bit
  - No parity
- Power-up the system.
- The terminal displays a message similar to the following:

```

Secondary MENMON for MEN PP01  2.3
-----
(c) 2004 - 2005 MEN mikro elektronik GmbH Nuernberg
      MENMON "Hurricane"
      Created Aug 29 2007  15:11:51
-----
| HW Revision: 03.01.01 | CPU: MPC5200 Rev. B3 |
| Serial Number: 1029 | Core/Mem Clock: 384 / 128.0 MHz |
| Board Model: | XLB/IPB Clock: 128 / 64.0 MHz |
| SDRAM: 128 MB | PCI Clock: 32.0 MHz |
| FRAM: 64 kB | PCI Slot: 0 ( SYSTEM ) |
| FLASH: 16 MB | RESET: POWER ON |
\-----/
Setting speed of NETIF 0 to AUTO

press 'ESC' for MENMON, 's' for setup
Setup network interface CLUN 0x02, 00:c0:3a:20:04:05 AUTO
Telnet daemon started on port 23
HTTP daemon started on port 80
MenMon>

```

- Now you can use the MENMON debugger (see detailed description in [Chapter 3 MENMON on page 31](#)).
- Observe the installation instructions for the respective software.

## 1.3 Installing Operating System Software

Operating software is programmed into the PP1's Flash memory. The PP1 supports Linux and VxWorks.

For a detailed description on how to install operating system software please refer to the respective documentation.



You can find any software available on MEN's [website](#).

## 2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned ([Chapter 6.1 Literature and Web Resources on page 48](#)).

### 2.1 Power Supply

The board is supplied with +5V and  $\pm 3.3V$  via PCI-104 connector J1. Supply voltages are monitored within the PPI. In case of power failure the CPU is held in reset state. The CPU operates at 1.5V core voltage and 3.3V memory I/O voltage. The core voltage is generated on the board from 3.3V.

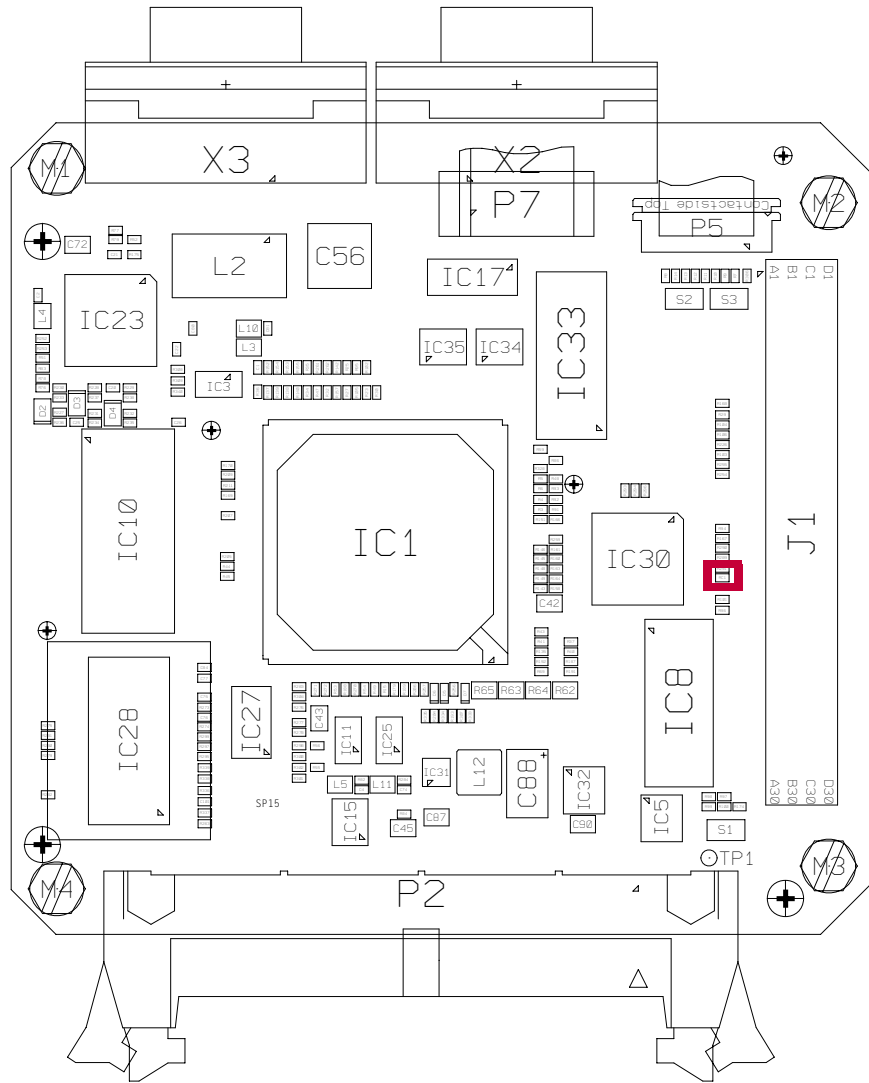
#### 2.1.1 Reset Control and Watchdog

A power control circuit inside the RTC generates a *PWROK* signal as soon as the 3.3V I/O voltage is stable. The reset CPLD then generates the initial *PORESET* signal to the CPU. The CPLD contains registers for reset cause detection.

The same CPLD includes a watchdog which supervises the correct function of the CPU. The watchdog timeout switches automatically from 50s after reset to 1.8s after the first trigger pulse. This allows a long watchdog timeout period during boot process.

For debug purposes the watchdog can be disabled by removing the configuration resistor RC1. In default configuration the resistor is assembled and the watchdog is active.

**Figure 2.** Position of watchdog configuration resistor RC1 on top side of the board



An additional hardware monitor (LM81) supervises 5V, 3.3V and 1.5V. It holds the CPU in Reset condition until all supply voltages are within their nominal values. Voltages are only supervised after program start-up, which means they are not monitored directly after power-up. The voltage limits can be verified by the CPU via I<sup>2</sup>C bus.

## **2.2 Temperature Sensor**

The PP1 provides a temperature sensor for in-system diagnosis. The LM81 is connected via the two-wire I<sup>2</sup>C interface (address 0x5E).

The temperature accuracy is -25°C to +100°C @ ±2°C (max.) and -55°C to +125°C @ ±3°C (max.).

The same device also monitors supply voltages as described in [Chapter 2.1.1 Reset Control and Watchdog on page 16](#).

## **2.3 Clock Supply**

A 32-MHz oscillator is used as the main clock source. This clock is internally multiplied to a 64-MHz SDRAM clock and XLB\_CLK. The XLB\_CLK is multiplied by another PLL to the 384-MHz core frequency.

The PCI and local bus interfaces operate at 32 MHz.

Two further oscillators provide the 48-MHz USB clock and 25-MHz Ethernet clock.

## **2.4 Real-Time Clock**

A battery-buffered real-time clock is integrated on the PP1 CPU board. It is accessed via I<sup>2</sup>C bus at address 0x00. The voltage of the snap hat standby battery is monitored by the RTC. A warning flag is set if the battery voltage falls below 2.5 V. The CPU can read this flag from bit D4 at word address 0x0F. After setting this flag the RTC continues operation for at least 1 month.

Interrupt generation of the RTC is not supported.

## **2.5 PowerPC CPU**

The board is equipped with the MPC5200 processor, which is based on a 400-MHz MPC603e core with an integrated double precision Floating Point Unit (FPU). The MPC5200 was designed for fast data throughput and processing, and for low power consumption. The integrated BestComm DMA controller offloads the main MPC603e core from I/O intensive data transfers. A PCI interface backed by the BestComm DMA controller and DDR support enables high-speed data transfers in and out of the MPC5200.

The PowerPC architecture, developed jointly by Motorola, IBM, and Apple Computer, is based on the POWER architecture implemented by the RS/6000™ family of computers. The PowerPC architecture takes advantage of recent technological advances in such areas as process technology, compiler design, and RISC microprocessor design to provide software compatibility across a diverse family of implementations, primarily single-chip microprocessors, intended for a wide range of systems.

## **2.6 Memory**

### **2.6.1 SDRAM**

The board provides 32 MB SDRAM on two memory components. It is organized as four memory banks.

### **2.6.2 Flash**

The board has on-board Flash. It is controlled by the MPC5200 and accommodates 16 MB. The data bus is 8 bits wide.

Flash memory contains the boot software for the MENMON/operating system bootstrapper and application software. The MENMON sectors are software-protected against illegal write transactions through a password in the serial download function of MENMON (cf. [Chapter 3.4 Updating Boot Flash on page 35](#)).

### **2.6.3 FRAM**

The board provides 64 KB non-volatile FRAM. The data bus is 8 bits wide.

The FRAM has a typical data retention of 10 years at +85°C.

### **2.6.4 EEPROM**

The board has a 16-kbit serial EEPROM for factory data, MENMON parameters, and for the VxWorks bootline.

## 2.7 Serial Ports COM1/COM2

The PP1 includes two independent RS232 interfaces. The first one (COM1) is controlled by the internal programmable serial controller PSC1 of the MPC5200. The second one (COM2) is controlled by PSC3.

Both interfaces are accessible at one 9-pin D-Sub connector at the front panel. The line drivers/receivers with 4 kV ESD protection are optically isolated.

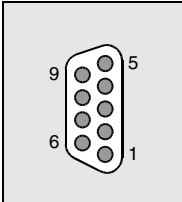
Please note that the connector has no standard RS232 pinout. It incorporates two RS232 interfaces. MEN offers an adapter for easy connection of two standard RS232 cables. See MEN's [website](#) for ordering information.

Both interfaces provide programmable baud rates up to 115.2 kbaud. Handshake lines are not supported.

Connector types:

- 9-pin D-Sub receptacle according to DIN41652/MIL-C-24308
- Mating connector:  
9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

**Table 1.** Pin assignment of 9-pin D-Sub COM1/COM2 connector

	9	COM2_TXD	5	GND
	8	-	4	-
	7	-	3	COM1_TXD
	6	-	2	COM1_RXD
	6	-	1	COM2_RXD

**Table 2.** Signal mnemonics for serial COM 1/2 port

Signal	Direction	Function
RXD	in	Receive data
TXD	out	Transmit data

### 2.7.1 Fuse Protection

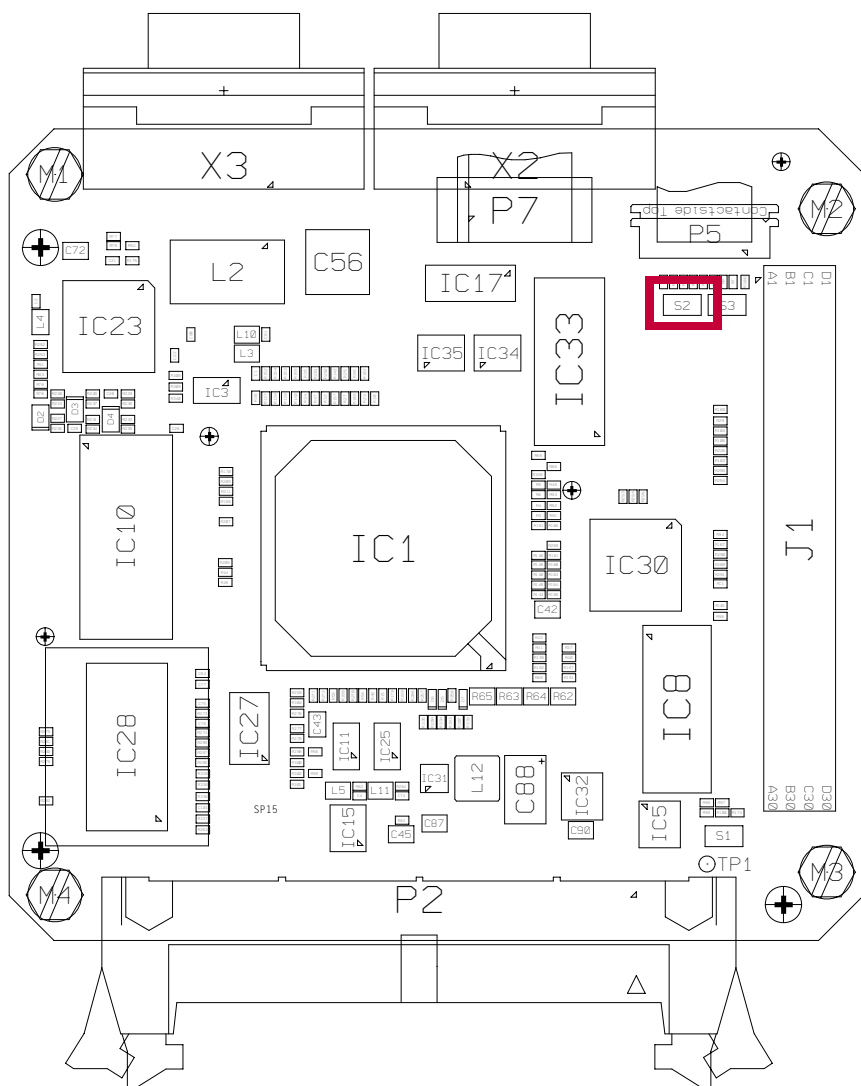


The RS232 interfaces are protected by a fuse. **This fuse is not intended to be exchanged by the customer. Your warranty for the PP1 will cease if you exchange the fuse on your own.** Please send your board to MEN for repair if a fuse blows.

- Current rating: 1.5A
- Type: fast
- Size: 1206
- MEN part number: 5675-0001

The fuse is located on the top side of PP1.

**Figure 3.** Position of fuse for COM protection on top side of the board



## 2.8 Ethernet

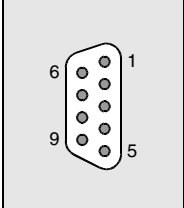
### 2.8.1 Implementation on PP1

The PP1 provides a fast Ethernet Interface. It is controlled by the MPC5200 internal fast Ethernet controller FEC. The Ethernet interface is accessible at a 9-pin D-Sub connector at the front panel.

Connector types:

- 9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:  
9-pin D-Sub receptacle according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

**Table 3.** Pin assignment of the 9-pin D-Sub Ethernet connector

	6	TPT-	1	TPT+
	7	-	2	-
	8	-	3	-
	9	TPR-	4	-
			5	TPR+

**Table 4.** Signal mnemonics for Ethernet 100Base-TX interface

Signal	Direction	Function
RX+/-	in	Differential pair of receive data lines
TX+/-	out	Differential pair of transmit data lines

## 2.8.2 General

Ethernet is a local-area network (LAN) protocol that uses a bus or star topology and supports data transfer rates of 100 Mbits/s and more. The Ethernet specification served as the basis for the IEEE 802.3 standard, which specifies the physical and lower software layers. Ethernet is one of the most widely implemented LAN standards.

Ethernet networks provide high-speed data exchange in areas that require economical connection to a local communication medium carrying bursty traffic at high-peak data rates.

A classic Ethernet system consists of a backbone cable and connecting hardware (e.g. transceivers), which links the controllers of the individual stations via transceiver (transmitter-receiver) cables to this backbone cable and thus permits communication between the stations.

## 2.8.3 10Base-T

10Base-T is one of several adaptations of the Ethernet (IEEE 802.3) standard for Local Area Networks (LANs). The 10Base-T standard (also called Twisted Pair Ethernet) uses a twisted-pair cable with maximum lengths of 100 meters. The cable is thinner and more flexible than the coaxial cable used for the 10Base-2 or 10Base-5 standards. Since it is also cheaper, it is the preferable solution for cost-sensitive applications.

Cables in the 10Base-T system connect with RJ45 connectors. A star topology is common with 12 or more computers connected directly to a hub or concentrator.

The 10Base-T system operates at 10 Mbits/s and uses baseband transmission methods.

## 2.8.4 100Base-T

The 100Base-T networking standard supports data transfer rates up to 100 Mbits/s. 100Base-T is actually based on the older Ethernet standard. Because it is 10 times faster than Ethernet, it is often referred to as Fast Ethernet. Officially, the 100Base-T standard is IEEE 802.3u.

There are several different cabling schemes that can be used with 100Base-T, e.g. 100Base-TX, with two pairs of high-quality twisted-pair wires.

## 2.9 I/O Connector – CAN Bus, USB, GPIO, Reset

The board features a 40-pin I/O connector (P2) that implements several interfaces:

- Two CAN interfaces (compatible with MEN’s SA-Adapters)
- USB port (compatible with MEN’s SA-Adapters)
- GPIO lines (PSC programmable serial controllers of MPC5200)  
(For more information see MPC5200 User Manual, [Chapter 6.1 Literature and Web Resources on page 48.](#))
- A reset and abort button<sup>1</sup>

Connector types 40-pin connector:

- 40-pin low-profile plug with lock, 2.54mm pitch, for ribbon-cable connection
- Mating connector:  
40-pin IDC receptacle, e.g. Elco Series 8290 IDC socket

MEN offers suitable adapters for easy connection of the USB and CAN interfaces. See MEN’s [website](#).



**Table 5. Pin assignment of the 40-pin I/O connector P2**

	1	PSC1[2]	2	PSC3[2]
	3	PSC1[3]	4	PSC3[3]
	5	PSC1[4]	6	PSC3[8]
	7	GND	8	+5V
	9	CAN2_TXD	10	CAN2_RXD
	11	-	12	-
	13	-	14	-
	15	-	16	-
	17	GND	18	+5V
	19	USB[0]	20	USB[1]
	21	USB[2]	22	USB[3]
	23	USB[4]	24	USB[5]
	25	USB[6]	26	USB[7]
	27	USB[8]	28	USB[9]
	29	PSC2[4]	30	TMR[7]
	31	GND	32	+5V
	33	CAN1_TXD	34	CAN1_RXD
	35	-	36	-
	37	ABORT#	38	GND
	39	RESET#	40	GND



<sup>1</sup> The abort button is implemented on the connector, but there is no actual button on the board. Please contact our sales staff if you need any help or extensions to use these interfaces.

**Table 6.** Signal mnemonics of 40-pin I/O connector P2

	Signal	Direction	Function
Power	+5V	-	+5V power supply, fuse-protected
	GND	-	Digital ground of respective interface
Button	ABORT#	in	Abort button
	RESET#	in	Reset button
CAN	CAN1_RXD	in	CAN1 receive data (TTL)
	CAN1_TXD	out	CAN1 transmit data (TTL)
	CAN2_RXD	in	CAN2 receive data (TTL)
	CAN2_TXD	out	CAN2 transmit data (TTL)
USB	USB[0]	out	OE – output enable
	USB[1]	out	TX_N – transmit negative
	USB[2]	out	TX_P – transmit positive
	USB[3]	in	RXD – receive data
	USB[4]	in	RX_P – receive positive
	USB[5]	in	RX_N – receive negative
	USB[6]	out	PORTPWR
	USB[7]	out	SPEED
	USB[8]	out	SUSPEND
	USB[9]	in	OVERCURRENT
GPIO/TMR	PSC1[2]	out	GPIO line (controlled by MPC5200 PSC1)
	PSC1[3]	out	GPIO line (controlled by MPC5200 PSC1)
	PSC1[4]	in/out	GPIO line (controlled by MPC5200 PSC1)
	PSC2[4]	in/out	GPIO line (controlled by MPC5200 PSC2)
	PSC3[2]	out	GPIO line (controlled by MPC5200 PSC3)
	PSC3[3]	out	GPIO line (controlled by MPC5200 PSC3)
	PSC3[8]	in	GPIO line (controlled by MPC5200 PSC3)
	TMR[7]	in/out	Timer 7 I/O line of MPC5200

### 2.9.1 CAN Bus

The PP1 provides two independent CAN interfaces. They are connected to the MSCAN controllers inside the MPC5200. The physical line interface is located on an SA-Adapter which must be attached to I/O connector P2.

The power pins of the CAN interfaces are protected by a fuse. See [Chapter 2.9.4 Fuse Protection on page 26](#).

### 2.9.2 USB

The PP1 provides one USB 1.1 port with a data rate of up to 12 Mbits/s. The USB controller is located inside the MPC5200. An external serial interface adapter (SA14) provides the physical interface and USB connector. You can also use the USB signals as GPIO lines, if needed.

The power pin of the USB interface is protected by a fuse. See [Chapter 2.9.4 Fuse Protection on page 26](#).

### 2.9.3 GPIO

The PP1 makes 8 GPIO lines of the MPC5200 accessible on the P2 I/O connector. These lines are completely user-configurable.

Please refer to the MPC5200 User Manual for details on how to control the signals. (See [Chapter 6.1 Literature and Web Resources on page 48](#).)

### 2.9.4 Fuse Protection

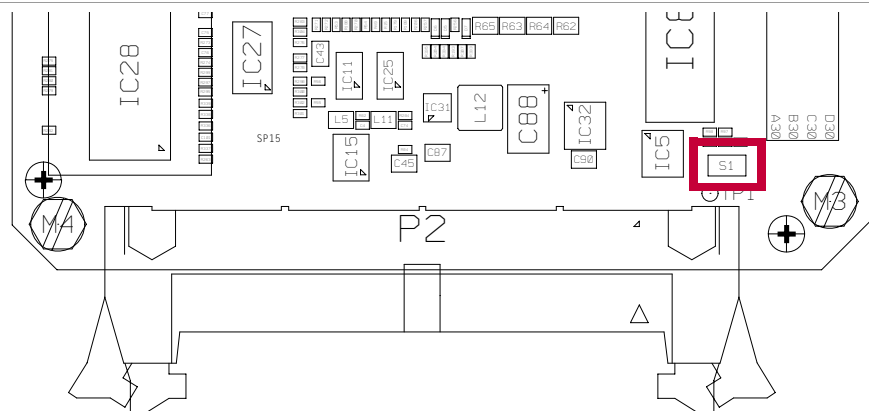


The power pins of the CAN and USB interfaces are protected by a fuse. **This fuse is not intended to be exchanged by the customer. Your warranty for the PP1 will cease if you exchange the fuse on your own.** Please send your board to MEN for repair if a fuse blows.

- Current rating: 3A
- Type: fast
- Size: 1206
- MEN part number: 5675-0003

The fuse is located on the top side of PP1.

**Figure 4.** Position of fuse for CAN bus and USB protection on top side of the board



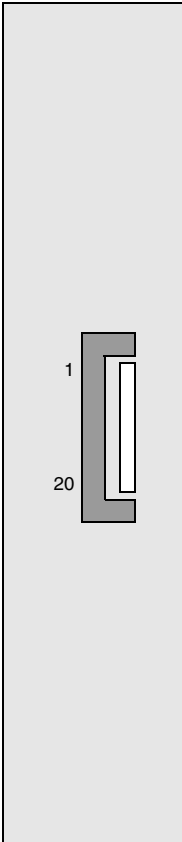
## 2.10 Alphanumerical Display

A 4-character alphanumerical display with push buttons and an LED can be connected to the PP1 via ribbon cable. The display is controlled by GPIO lines of the MPC5200.

Connector type:

- 20-pin ZIF receptacle, 0.5mm pitch, for ribbon-cable connection

**Table 7.** Pin assignment of the 20-pin display connector

	1	+5V
	2	+5V
	3	+5V
	4	+5V
	5	TMR0
	6	GND
	7	TMR1
	8	GND
	9	TMR2
	10	GND
	11	TMR3
	12	GND
	13	TMR4
	14	GND
	15	TMR5
	16	GND
	17	TMR6
	18	GND
	19	MRESET#
	20	GND

**Table 8.** Signal mnemonics for display interface

Signal	Direction	Function
+5V	-	+5V power supply, fuse-protected
GND	-	Ground
MRESET#	in	Manual reset
TMR0	out	Clock
TMR1	out	Data out
TMR2	out	Chip select
TMR3	in	Data in
TMR4	out	LED
TMR5	in	Push button S1
TMR6	in	Push button S2

### 2.10.1 Fuse Protection

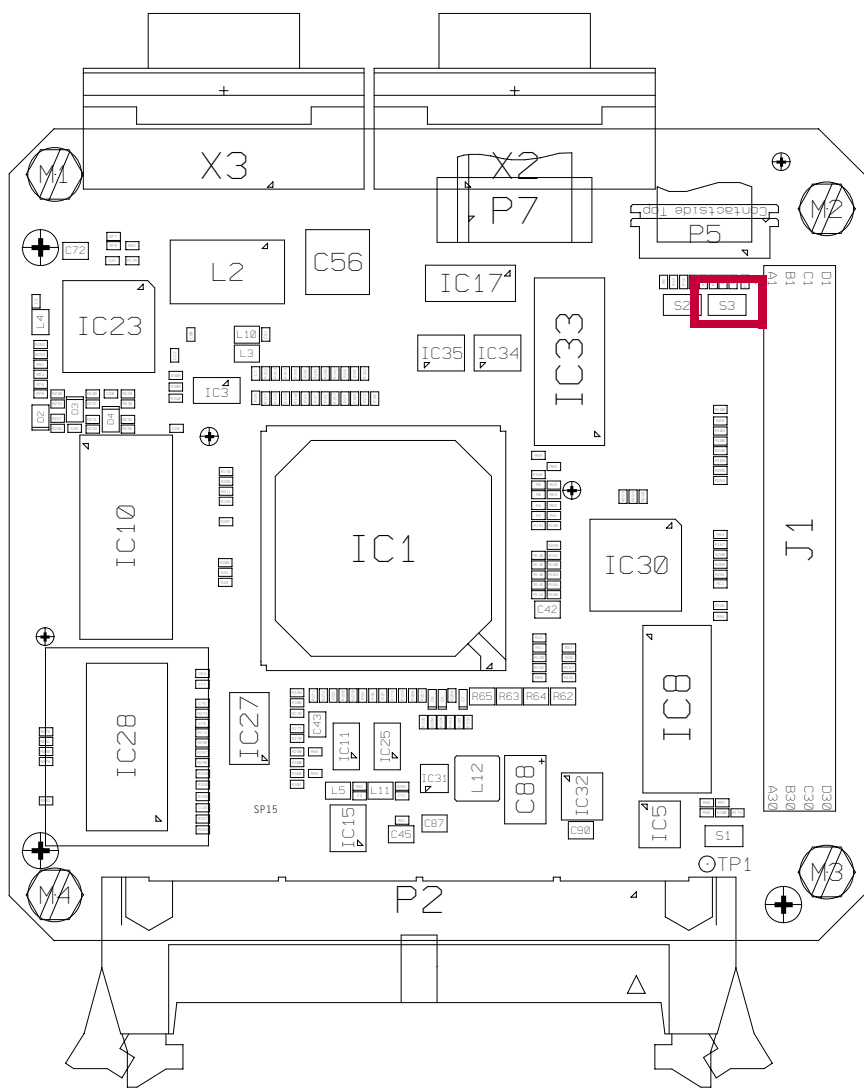


The power pins of the display interface are protected by a fuse. **This fuse is not intended to be exchanged by the customer. Your warranty for the PP1 will cease if you exchange the fuse on your own.** Please send your board to MEN for repair if a fuse blows.

- Current rating: 3A
- Type: fast
- Size: 1206
- MEN part number: 5675-0003

The fuse is located on the top side of PP1.

**Figure 5.** Position of fuse for display protection on top side of the board



## 2.11 PCI-104 Interface J1

The PP1 provides a 32-bit/33-MHz PCI interface at the PCI-104 connector J1. The PP1 is always the system controller of the PCI-104 bus and supports one external master.

The VI/O signaling voltage is +3.3 V, the board is not 5 V tolerant.

Connector types:

- 4-row, 120-pin PCI-104 receptacle connector, 2mm pitch, e.g. Samtec ESQT-130-02-G-Q-368
- Mating connector:  
4-row, 120-pin PCI-104 plug connector, 2mm pitch

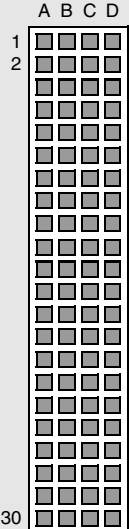
Note: Signals shown in grey color are not used.

**Table 9.** Mnemonics of special signals of PCI J1

Signal	Direction	Function
+5V	-	+5V supply
SCK	out	SPI clock
SCS1, SCS2	out	SPI chip select 1 and 2
SDI	in	SPI data in
SDO	out	SPI data out

For a description of signals please refer to the PCI-104 specification see [Chapter 6.1 Literature and Web Resources](#) on page 48.

**Table 10.** Pin assignment of PCI J1

		A	B	C	D
	1	SCS1	SCS2	+5V	AD00
	2	+3.3V	AD02	AD01	+5V
	3	AD05	GND	AD04	AD03
	4	C/BE0#	AD07	GND	AD06
	5	GND	AD09	AD08	GND
	6	AD11	+3.3V	AD10	M66EN
	7	AD14	AD13	GND	AD12
	8	+3.3V	C/BE1#	AD15	+3.3V
	9	SERR#	GND	IIC SDA	PAR
	10	GND	PERR#	+3.3V	IIC SCK
	11	STOP#	+3.3V	LOCK#	GND
	12	+3.3V	TRDY#	GND	DEVSEL#
	13	FRAME#	GND	IRDY#	+3.3V
	14	GND	AD16	+3.3V	C/BE2#
	15	AD18	+3.3V	AD17	GND
	16	AD21	AD20	GND	AD19
	17	+3.3V	AD23	AD22	+3.3V
	18	IDSEL0	GND	IDSEL1	IDSEL2
	19	AD24	C/BE3#	+3.3V	IDSEL3
	20	GND	AD26	AD25	GND
	21	AD29	+5V	AD28	AD27
	22	+5V	AD30	GND	AD31
	23	REQ0#	GND	REQ1#	+3.3V
	24	GND	REQ2#	+5V	GNT0#
	25	GNT1#	VI/O	GNT2#	GND
	26	+5V	CLK0	GND	CLK1
	27	CLK2	+5V	CLK3	GND
	28	GND	INTD#	+5V	RST#
	29	+12V	INTA#	INTB#	INTC#
	30	-12V	SCK	SDO	SDI

## 3 MENMON

### 3.1 General

MENMON is the CPU board firmware that is invoked when the system is powered on.

The basic tasks of MENMON are:

- Initialize the CPU and its peripherals.
- PCI auto configuration.
- Perform self-test.
- Provide debug/diagnostic features on MENMON command line.
- Boot operating system.
- Update firmware or operating system.



The following description only includes board-specific features. For a general description and in-depth details on MENMON 3.x, please refer to the [MENMON 2nd Edition User Manual](#).

### 3.1.1 State Diagram

Figure 6. MENMON – State Diagram, Degraded Mode/Full Mode

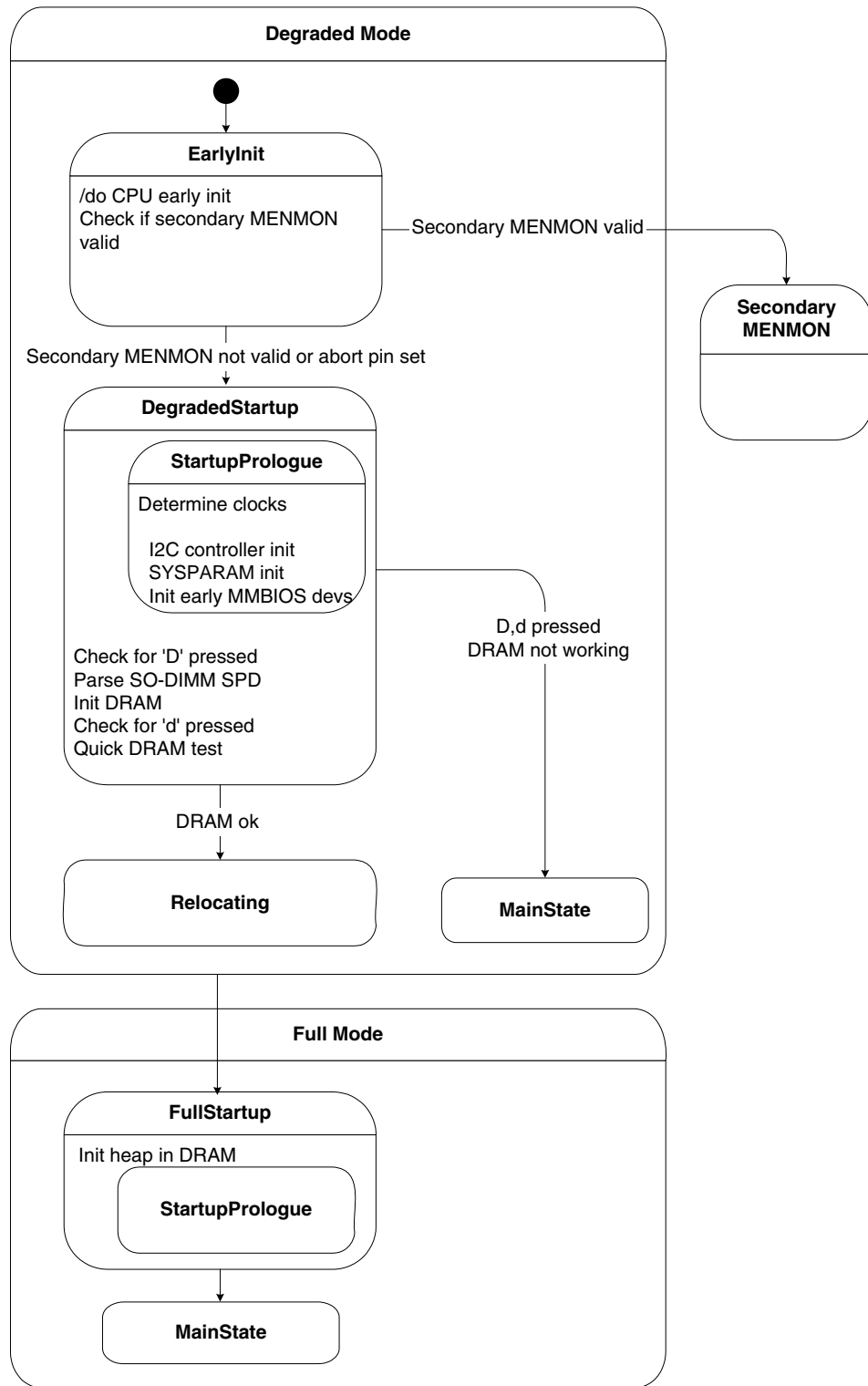
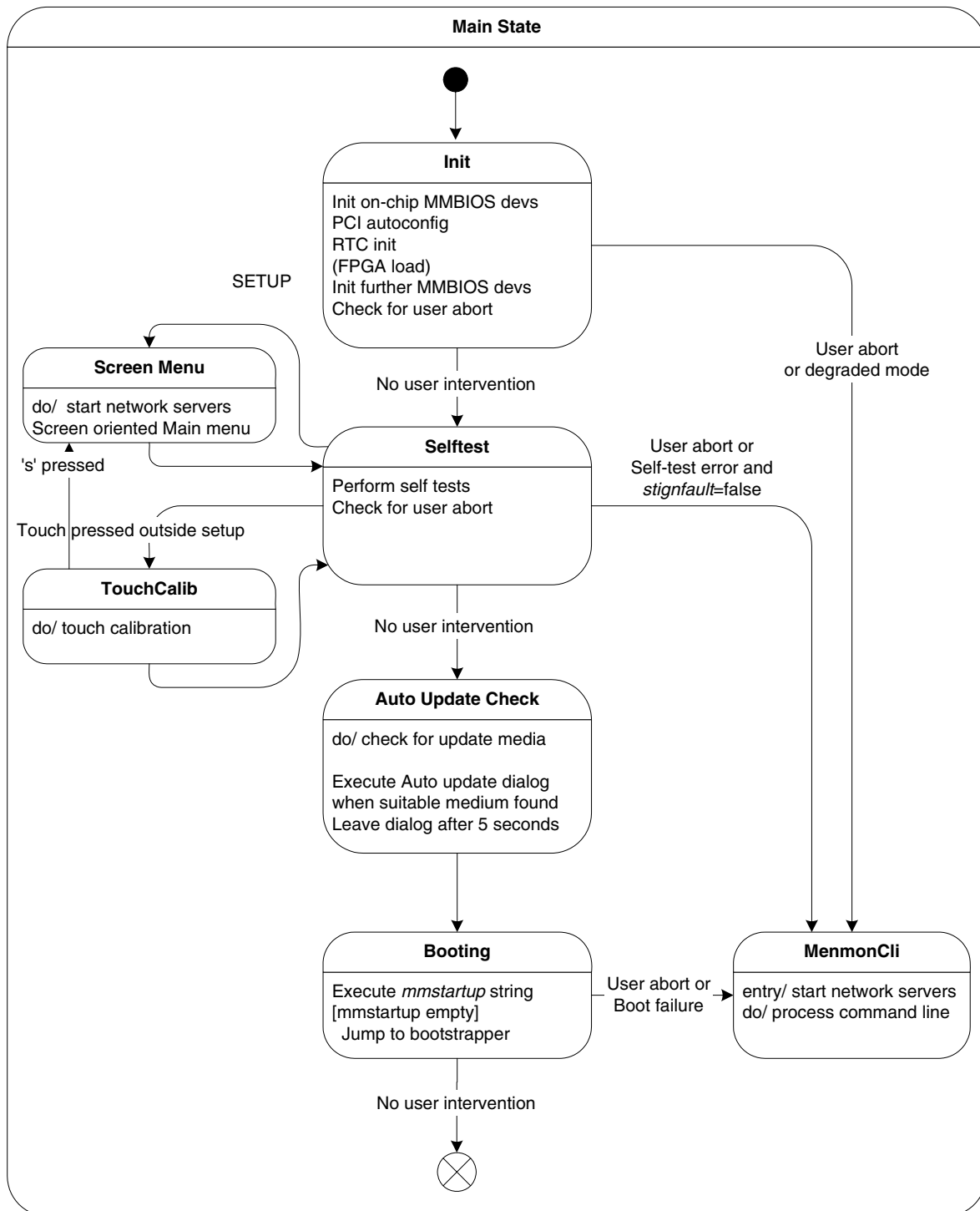


Figure 7. MENMON – State Diagram, Main State



## 3.2 Interacting with MENMON

To interact with MENMON, you can use the following consoles:

- COM1/2 serial interfaces
- Telnet via network connection
- HTTP monpage via network connection

The default setting of the COM ports is 115,200 baud, 8 data bits, no parity, and one stop bit.

### 3.2.1 Entering the Setup Menu/Command Line

During normal boot, you can abort the booting process in different ways during the self-test, depending on your console:

- With a touch panel press the "Setup" button to enter the Setup Menu.
- With a text console press the "s" key to enter the Setup Menu.
- With a text console press "ESC" to enter the command line.

By default, the self-test is not left until 3 seconds have elapsed (measured from the beginning of the self-test), even if the actual test has finished earlier, to give the user a chance to abort booting and enter the Setup Menu.

## 3.3 Configuring MENMON for Automatic Boot

You can configure how MENMON boots the operating system either through the Setup Menu or through the command line.

In the Basic Setup Menu you can select the boot sequence for the bootable devices on the PP1. The selected sequence is stored in system parameter *mmstartup* as a string of MENMON commands. For example, if the user selects: "Ether, (None)", the *mmstartup* string will be set to "NBOOT TFTP".

You can view and modify this string directly, using the Expert Setup Menu, option *Startup string*, or through the command-line command *EE-MMSTARTUP*.



(See also [MENMON 2nd Edition User Manual](#) for further details.)

### 3.4 Updating Boot Flash

Primary MENMON is hardware protected.

Please note that MENMON 3.x as primary MENMON cannot start older versions as secondary (because older versions do not appear to have a valid header).

#### 3.4.1 Update via the Serial Console using *SERDL*

You can use command *SERDL* to update program data using the serial console.

The following table shows the PP1 locations:

**Table 11.** MENMON – Program Update Files and Locations

File Name Extension	Typical File Name	Password for <i>SERDL</i>	Location
.PMM	14PP01-00_02_03.PMM	PMENMON	Primary MENMON
.SMM	14PP01-00_02_03.SMM	MENMON	Secondary MENMON
.Fxxx	MYFILE.F000	-	Starting at sector xxx in boot Flash
.Exx	MYFILE.E00	-	Starting at byte xx (decimal) in EEPROM

#### 3.4.2 Update from Network using *NDL*

You can use the network download command *NDL* to download the update files from a TFTP server in network. The file name extensions, locations and passwords are the same as for the *SERDL* command.

### 3.5 Diagnostic Tests

**Table 12.** MENMON – Diagnostic tests

<b>Test Name</b>	<b>Description</b>	<b>Availability</b>
<i>EEPROM</i>	I2C access/Magic nibble check Groups: POST AUTO	Always
<i>SDRAM</i>	Quick SDRAM connection test Groups: POST AUTO	Always
<i>RTC</i>	RTC access test Groups: POST AUTO	Always
<i>IWDOG</i>	Processor watchdog test Groups: POST AUTO	Always
<i>LM81</i>	Voltage supervisor test Groups: POST AUTO	Always
<i>EWDOG</i>	PLD watchdog test Groups: POST AUTO	Always
<i>CHECKSUM PMM</i>	Checksum Primary MENMON Groups: POST AUTO	Always
<i>CHECKSUM SMM</i>	Checksum Secondary MENMON Groups: POST AUTO	Always

## 3.6 MENMON Configuration and Organization

### 3.6.1 Consoles

You can select the active consoles by means of system parameters *con0..con3*:

**Table 13.** MENMON – System Parameters for Console Selection

Parameter (alias)	Description	Default	User Access
<i>con0..con3</i>	CLUN of console 0..3. CLUN=0x00: disable CLUN=0xFF: Autoselect next available console <i>con0</i> is implicitly the debug console	<i>con0</i> : 08 (COM1) <i>con1</i> : FF (auto) <i>con2</i> : 00 (none) <i>con3</i> : 00 (none)	Read/write
<i>gcon</i>	CLUN of graphics device to display boot logo CLUN=0x00: disable CLUN=0xFF: Autoselect first available graphics console	0xFF (AUTO)	Read/write

## 3.6.2 MENMON Memory Map

### 3.6.2.1 MENMON Memory Address Mapping

**Table 14.** MENMON – Address Map (Full-featured mode)

Address Space	Size	Description
0x 0000 0000 .. 0000 1400	5 KB	Exception vectors
0x 0000 3000 .. 0000 3FFF	4 KB	MENMON parameter string
0x 0000 4200 .. 0000 42FF	100 bytes	VxWorks bootline
0x 0000 4300 .. 00FF FFFF	Nearly 16 MB	Free
0x 0100 0000 .. 01EF FFFF	15 MB	Free or download area
0x 01F0 0000 .. 01F7 FFFF	512 KB	Text + Reloc
0x 01F8 0000 .. 01F8 FFFF	64 KB	Stack
0x 01F9 0000 .. 01F9 FFFF	64 KB	Stack for user programs and operating system boot
0x 01FA 0000 .. 01FE FFFF	384 KB	Heap
0x 01FF 0000 .. 01FF FFFF	64 KB	Not touched for OS post mortem buffer i.e. VxWorks WindView or MDIS debugs
0x 0200 000 .. End of RAM		Free or download area

### 3.6.2.2 Boot Flash Memory Map

**Table 15.** MENMON – Boot Flash Memory Map (16 MB)

Address Space	Description
0x FF00 0000 .. FF7F FFFF	First 8 MB of 16 MB Flash free
0x FF80 0000 .. FFEF FFFF	Free
0x FFF0 0000 .. FF7F FFFF	Primary MENMON
0x FFF8 0000 .. FFFF FFFF	Secondary MENMON

### 3.6.3 MENMON BIOS Logical Units

The following table shows fixed assigned CLUNs. All other CLUNs are used dynamically.

**Table 16.** MENMON – Controller Logical Units (CLUNs)

CLUN	MENMON BIOS Name	Description
0x02	ETHER0	On-board FEC5200 Ethernet
0x08	COM1	MPC5200 PSC1 channel #0
0x20		All other devices dynamically detected on PCI or FPGA devices
0x40		Telnet console
0x41		HTTP monitor console

**Table 17.** MENMON – Device Logical Units (DLUNs)

CLUN/DLUN	MENMON BIOS Name	Description
2/2	ETHER0	Ethernet
8/8	COM1	COM1

### 3.6.4 System Parameters

System parameters are parameters stored in EEPROM. Some parameters are automatically detected by MENMON (such as CPU type and frequency). The parameters can be modified through the *EE-xxx* command via the command line.

#### 3.6.4.1 Backward Compatibility of Parameters

MENMON 3.x for the PP1 is backward-compatible to older MENMON versions:

- Existing EEPROM sections are kept unchanged.
- A new EEPROM section (*memmx\_parms*) has been added at offset 0x200..0x240, which mainly stores the network and console configuration.
- A new EEPROM section (*kerpar*) has been added at offset 0x240..0x440 to store Linux kernel parameters.

#### 3.6.4.2 PP1 System Parameters

A blue background marks parameters different/new to older MENMON versions.

**Table 18.** MENMON – PP1 system parameters

Parameter (alias)	Description	Standard Default	Parameter String <sup>1</sup>	User Access
<b>Autodetected Parameters</b>				
<i>mem0</i>	RAM size (decimal, kilobytes)		Yes	Read-only
<i>flash0</i>	Boot Flash size (decimal, kilobytes)		Yes	Read-only
<i>cpu</i>	CPU type as ASCII string (e.g. "MPC5200")		Yes	Read-only
<i>cpuclockhz</i>	CPU core clock frequency (decimal, Hz)		Yes	Read-only
<i>inclkhz</i>	CPU input clock frequency (decimal, Hz)		Yes	Read-only
<i>memclkhz</i>	Memory clock frequency (decimal, Hz)		Yes	Read-only
<i>xlbclockhz</i>	XBL bus clock frequency (decimal, Hz)		Yes	Read-only
<i>ipbclockhz</i>	IPB bus clock frequency (decimal, Hz)		Yes	Read-only
<i>pciclockhz</i>	PCI bus clock frequency (decimal, Hz)		Yes	Read-only
<i>clun</i>	MENMON controller unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
<i>dlun</i>	MENMON device unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
<i>rststat</i>	Reset status code as a string, see <a href="#">Chapter 3.6.4.3 Parameter rststat (Reset Cause)</a> on page 42		Yes	Read-only
<i>mmst</i>	Status of diagnostic tests, as a string		Yes	Read-only

Parameter (alias)	Description	Standard Default	Parameter String <sup>1</sup>	User Access
<i>mm</i>	Info whether primary or secondary MENMON has been used for booting, either "smm" or "pmm"		Yes	Read-only
<b>Production Data</b>				
<i>brd</i>	Board name	-	Yes	Read-only
<i>brdmod</i>	Board model "mm"	-	Yes	Read-only
<i>brdrev</i>	Board revision "xx.yy.zz"	-	Yes	Read-only
<i>sernbr</i>	Board serial number	-	Yes	Read-only
<i>prodat</i>	Board production date MM/DD/YYYY	-	Yes	Read-only
<i>repmat</i>	Board last repair date MM/DD/YYYY	-	Yes	Read-only
<b>MENMON Persistent Parameters</b>				
<i>con0..conN</i>	CLUN of console 0..n. (hex) (see <a href="#">Chapter 3.6.1 Consoles on page 37</a> )	0x08	No	Read/write
<i>gcon</i>	CLUN of graphics screen (hex) (see <a href="#">Chapter 3.6.1 Consoles on page 37</a> )	0xFF = auto	No	Read/write
<i>cbr (baud)</i>	Baudrate of all UART consoles (dec)	115200	Yes	Read/write
<i>bsadr (bs)</i>	Bootstrapper address. Used when <i>BO</i> command was called without arguments. (hexadecimal, 32 bits)	0	No	Read/write
<i>ecl</i>	CLUN of attached network interface (hex)	0xFF	No	Read/write
<i>tto</i>	Minimum timeout between network retries (decimal, in seconds)	0	No	Read/write
<i>tries</i>	Number of network tries	20	No	Read/write
<i>tdp</i>	Telnet server TCP port (decimal)	-1	No	Read/write
<i>hdp</i>	HTTP server TCP port (decimal)	-1	No	Read/write
<i>stignfault</i>	Ignore POST failure, continue boot (bool)	0	No	Read/write
<i>stdisXXX</i>	Disable POST test XXX (bool)	0	No	Read/write
<i>stwait</i>	Time in 1/10 seconds to stay at least in SELFTEST state (decimal) 0 = Continue as soon as POST has finished	10	No	Read/write
<i>mmstartup (startup)</i>	Start-up string (511 chars max)	Empty string	No	Read/write
<i>kerpar</i>	Linux Kernel Parameters (399 chars max)	Empty string	No	Read/write
<i>u00..u15</i>	User parameters (hex, 16 bits)	0x0000	No	Read/write

Parameter (alias)	Description	Standard Default	Parameter String <sup>1</sup>	User Access
<i>useflpar</i>	Store <i>kerpar</i> and <i>mmstartup</i> parameters in boot Flash rather than in EEPROM (bool)	0	No	Read/write
<i>nmac0</i>	MAC address of Ethernet interface 0. Format e.g. "00112233445566".	0x00C03A200000	Yes	Read/write
<i>nspeed0</i>	Speed setting for Ethernet interface 0. Possible values: <i>AUTO</i> , <i>10HD</i> , <i>10FD</i> , <i>100HD</i> , <i>100FD</i>	AUTO	Yes	Read/write
<b>VxWorks Bootline Parameters</b>				
<i>bf (bootfile)</i>	Boot file name (127 chars max)	Empty string	No	Read/write
<i>e (netip)</i>	IP address, subnet mask, e.g. 192.1.1.28:ffffff00	Empty string	No	Read/write
<i>netaddr</i>	Access the IP address part of <i>netip</i> parameter		No	Read/write
<i>netsm</i>	Access the subnet mask part of <i>netip</i> parameter		No	Read/write
<i>h (nethost)</i>	Host IP address (used when booting over <i>NBOOT TFTP</i> )	Empty string	No	Read/write
<i>g (netgw)</i>	IP address of default gateway	Empty string	No	Read/write
<i>tn (netname)</i>	Host name of this machine	Empty string	No	Read/write
<i>s</i>	VxWorks start-up script	Empty string	No	Read/write
<i>bootdev</i>	VxWorks boot device name	Empty string	No	Read/write
<i>unitnum</i>	VxWorks boot device unit number (decimal)	0	No	Read/write
<i>procnum</i>	VxWorks processor number (decimal)	0	No	Read/write
<i>hostname</i>	VxWorks name of boot host	Empty string	No	Read/write

<sup>1</sup> Parameters marked by "Yes" are part of the MENMON parameter string.

### 3.6.4.3 Parameter *rststat* (Reset Cause)

The following *rststat* values are possible:

When MENMON starts up, it determines the reset cause and sets system parameter *rststat* accordingly:

**Table 19.** MENMON – Reset Causes through System Parameter *rststat*

<i>rststat</i> Value	Description
<i>hrst</i>	Board was reset due to activation of HRESET line
<i>pwon</i>	Power On
<i>pdrop</i>	Power error
<i>wdog</i>	Board was reset by watchdog timer unit
<i>rbut</i>	Board was reset by an external reset pin (e.g. reset button)

### 3.7 MENMON Commands

The following table gives all MENMON commands that can be entered on the PP1 MENMON prompt.

**Table 20.** MENMON – Command Reference

Command	Description
.[<reg>] [<val>]	Display/modify registers in debugger model
ARP	Dump network stack ARP table
AS <addr> [<cnt>]	Assemble memory
B[DC#] [<addr>]	Set/display/clear breakpoints
BIOS_DBG <mask> [net]   cons <clun>	Set MENMON BIOS or network debug level, set debug console
BO [<addr>] [<opts>]	Call OS bootstrapper
BOOTP [<opts>]	Obtain IP config via BOOTP
C[BWLLNAX#] <addr> [<val> ...]	Change memory
CONS	Show active consoles
CONS-ACT <clun1> [<clun2>] ...	Test console configuration
D [<addr>] [<cnt>]	Dump memory
DBOOT [<clun>] [<dlun>] [<opts>]	Boot from disk
DCACHE OFFION	Enable/disable data cache
DI [<addr>] [<cnt>]	Disassemble memory
DIAG [<which>] [VTF]	Run diagnostic tests
DSKWR <args>	Write blocks to RAW disk
DSKRD <args>	Read blocks from RAW disk
EER[-xxx] [<arg>]	Raw serial EEPROM commands
EE[-xxx] [<arg>]	Persistent system parameter commands
ERASE <D> [<O>] [<S>]	Erase Flash sectors
ESMCB-xxx	ESM carrier commands
FI <from> <to> <val>	Fill memory (byte)
GO [<addr>]	Jump to user program
H HELP	Print help
I [<D>]	List board information
ICACHE OFFION	Enable/disable instruction cache
IOI	Scan for BIOS devices
LOGO	Display MENMON start-up screen
LS <clun> <dlun> [<opts>]	List files/partitions on device
MC <addr1> <addr2> <cnt>	Compare memory
MII <clun> [<reg>] [<val>]	Ethernet MII register command

Command	Description
MO <from> <to> <cnt>	Move (copy) memory
MS <from> <to> <val>	Search pattern in memory
MT [<opts>] <start> <end> [<runs>]	Memory test
NBOOT [<opts>]	Boot from Network
NDL [<opts>]	Update Flash from network
NETSTAT	Show current state of networking parameters
PCI-VPD[-] <devNo> [<busNo>] [<capId>]	PCI Vital Product Data dump
PCIC <dev> <addr> [<bus>] [<func>]	PCI config register change
PCID[+] <dev> [<bus>] [<func>]	PCI config register dump
PCI	PCI probe
PCIR	List PCI resources
PFLASH <D> <O> <S> [<A>]	Program Flash
PGM-XXX <args>	Media copy tool
PING <host> [<opts>]	Network connectivity test
RST	Cause an instant system reset
RTC[-xxx] [<arg>]	Real time clock commands
S [<addr>]	Single step user program
SERDL [<passwd>]	Update Flash using YModem protocol
SETUP	Open Setup Menu

## 4 Organization of the Board

To install software on the board or to develop low-level software it is essential to be familiar with the board's address and interrupt organization.

### 4.1 Memory Mappings

**Table 21.** Memory Map – Processor View

CPU Address Range	Size	Description
0x 0000 0000 .. 01FF FFFF	32MB	SDRAM
0x 8000 0000 .. BFFF FFFF	1GB	PCI Memory Space
0x F000 0000		MPC5200 internal SRAM and Registers
0x F200 0000 .. F200 FFFF	64KB	FRAM (CS2)
0x F400 0000 .. F400 FFFF	64KB	CPLD (CS1)
0x FD00 0000 .. FDFE FFFF	16MB	PCI ISA Memory Space
0x FE00 0000 .. FE00 FFFF	64KB	PCI I/O / Config Space <sup>1</sup>
0x FF00 0000 .. FFFF FFFF	16MB	Flash (CS0)

<sup>1</sup> Note: I/O Space and Config Space can be accessed at the same time.

**Table 22.** Memory Map – PCI View

Address Range	Size	Description
0x 4000 0000 .. 7FFF FFFF	1GB	PCI/SDRAM (enabled)

**Table 23.** BATS set up by MENMON<sup>1</sup>

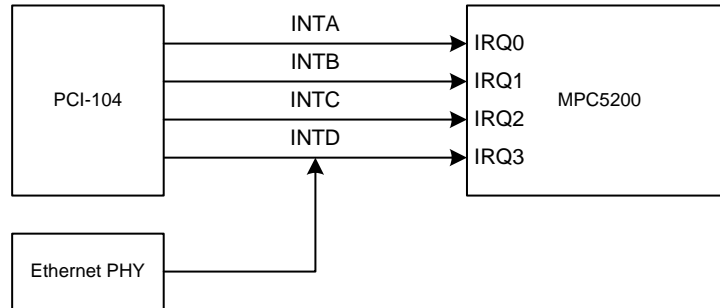
BAT	Address	Description
DBAT 0	0x F000 0000 .. FFFF FFFF	ROM / I/O non cacheable
IBAT 0	0x F000 0000 .. FFFF FFFF	ROM / I/O cacheable
DBAT 1	0x 0000 0000 .. 0FFF FFFF	DRAM non cacheable
IBAT 1	0x 0000 0000 .. 0FFF FFFF	DRAM cacheable
DBAT 2	0x 8000 0000 .. 8FFF FFFF	PCI MEM non cacheable
IBAT 2	0x 8000 0000 .. 8FFF FFFF	PCI MEM non cacheable
DBAT/IBAT 3..7	Disabled	

<sup>1</sup> Unless otherwise stated, all BATS are initialized with W I M !G.

## 4.2 Interrupt Handling

The following figure shows how interrupts are routed on PP1.

**Figure 8.** Interrupt Handling



## 4.3 SMB Devices

**Table 24.** SMB Devices

Address	Function
0x5E	LM81
0xA0..0xAE	EEPROM
0xD0	RTC

## 5 Maintenance

### 5.1 Lithium Battery

The PP1 contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced!

Replace only with the same or equivalent type:

- Manufacturer: ST
- Type: M4T32-BR12SH6
- Capacity: 120mAh

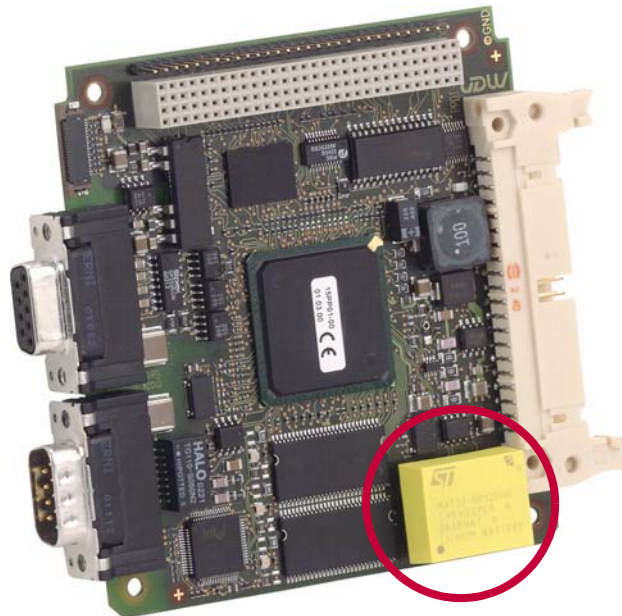
Data retention time is mainly a function of temperature and power duty cycle. At a temperature of +25°C, the battery life can be expected to be greater than 10 years without system power.

To replace the battery, simply unplug it from its socket and install a new battery. The socket is protected against reverse connection, so that the battery will fit into the socket only if properly aligned.



**Caution:** To avoid draining battery do **not** place snap hat pins in a conductive foam. Dispose of used batteries according to the manufacturer's instructions!

*Figure 9. Position of Lithium Battery on PP1*



## 6 Appendix



### 6.1 Literature and Web Resources

- PP1 data sheet with up-to-date information and documentation:  
[www.men.de](http://www.men.de)

#### 6.1.1 PCI-104

- PCI-104:  
PCI-104 Specification; PC/104 Embedded Consortium  
[www.pc104.org](http://www.pc104.org)

#### 6.1.2 PowerPC Processor

- MPC5200:  
MPC5200 User Manual  
MPC5200UM/D; 2003; Motorola, Inc.  
[www.motorola.com/PowerPC](http://www.motorola.com/PowerPC)

#### 6.1.3 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE  
[www.ieee.org](http://www.ieee.org)
- Charles Spurgeon's Ethernet Web Site  
Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.  
[www.ethermanage.com/ethernet/](http://www.ethermanage.com/ethernet/)
- InterOperability Laboratory, University of New Hampshire  
This page covers general Ethernet technology.  
[www.iol.unh.edu/services/testing/ethernet/training/](http://www.iol.unh.edu/services/testing/ethernet/training/)

#### 6.1.4 USB

- USB:  
Universal Serial Bus Specification Revision 1.0; 1996; Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom  
[www.usb.org](http://www.usb.org)

#### 6.1.5 Hardware Monitor

- LM81:  
[www.national.com](http://www.national.com)

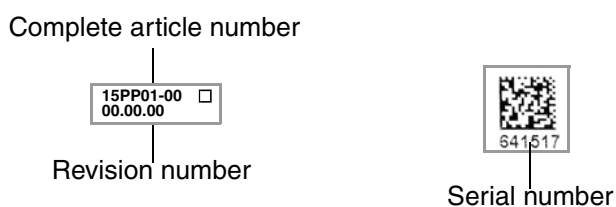
## 6.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the PPI. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

**Figure 10.** Labels giving the board's article number, revision and serial number



You can request the circuit diagrams for the current revision of the product described in this manual by completely filling out and signing the following non-disclosure agreement.

Please send the agreement to MEN by mail. We will send you the circuit diagrams along with a copy of the completely signed agreement by return mail.

MEN reserves the right to refuse sending of confidential information for any reason that MEN may consider substantial.



# Non-Disclosure Agreement

for Circuit Diagrams provided by MEN Mikro Elektronik GmbH

between

MEN Mikro Elektronik GmbH  
Neuwieder Straße 5-7  
D-90411 Nürnberg

("MEN")

and

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

("Recipient")

We confirm the following Agreement:

**MEN**

Date: \_\_\_\_\_

Name: \_\_\_\_\_

Function: \_\_\_\_\_

**Recipient**

Date: \_\_\_\_\_

Name: \_\_\_\_\_

Function: \_\_\_\_\_

Signature:

\_\_\_\_\_

Signature:

\_\_\_\_\_

The following Agreement is valid as of the date of the MEN signature.

MEN Mikro Elektronik GmbH

Neuwieder Straße 5-7  
90411 Nürnberg  
Deutschland

Tel. +49-911-99 33 5-0  
Fax +49-911-99 33 5-901

E-Mail [info@men.de](mailto:info@men.de)  
[www.men.de](http://www.men.de)

## 1 Subject

The subject of this Agreement is to protect all information contained in the circuit diagrams of the following product:

**Article Number:** \_\_\_\_\_ [filled out by recipient]

MEN provides the recipient with the circuit diagrams requested through this Agreement only for information.



## 2 Responsibilities of MEN

Information in the circuit diagrams has been carefully checked and is believed to be accurate as of the date of release; however, no responsibility is assumed for inaccuracies. MEN will not be liable for any consequential or incidental damages arising from reliance on the accuracy of the circuit diagrams. The information contained therein is subject to change without notice.

## 3 Responsibilities of Recipient

The recipient, obtaining confidential information from MEN because of this Agreement, is obliged to protect this information.

The recipient will not pass on the circuit diagrams or parts thereof to third parties, neither to individuals nor to companies or other organizations, without the written permission by MEN. The circuit diagrams may only be passed to employees who need to know their content. The recipient protects the confidential information obtained through the circuit diagrams in the same way as he protects his own confidential information of the same kind.

## 4 Violation of Agreement

The recipient is liable for any damage arising from violation of one or several sections of this Agreement. MEN has a right to claim damages amounting to the damage caused, at least to €100,000.

## 5 Other Agreements

MEN reserves the right to pass on its circuit diagrams to other business relations to the extent permitted by the Agreement.

Neither MEN nor the recipient acquire licenses for the right of intellectual possession of the other party because of this Agreement.

This Agreement does not result in any obligation of the parties to purchase services or products from the other party.

## 6 Validity of Agreement

The period after which MEN agrees not to assert claims against the recipient with respect to the confidential information disclosed under this Agreement shall be \_\_\_\_\_ months [filled out by MEN]. (Not less than twenty-four (24) nor more than sixty (60) months.)

## 7 General

If any provision of this Agreement is held to be invalid, such decision shall not affect the validity of the remaining provisions and such provision shall be reformed to and only to the extent necessary to make it effective and legal.

This Agreement is only effective if signed by both parties.

Amendments to this Agreement can be adopted only in writing. There are no supplementary oral agreements.

This Agreement shall be governed by German Law.

The court of jurisdiction shall be Nuremberg.

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