

IO104-60IN Manual

Manufactured by
TRI-M ENGINEERING

Engineered Solutions for Embedded Applications

Technical Manual

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PREFACE

This manual is for integrators of applications of embedded systems. It contains information on hardware requirements and interconnection to other embedded electronics.

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FEATURES

- 60 opto-isolated inputs.
- Inputs on standard 0.1" pitch 40 pin headers.
- I/O access to inputs through I/O memory mapped registers via PC/104 bus.
- All inputs are opto-isolated.
- Input Range 3V to 24 V AC or DC input.
- Multiple IO104-60IN boards can be stacked.
- Temperature Range -40 to 85C.
- PC/104 compliant, 3.75" X 3.55".
- Weight: 2.27 oz / 64 grams.

Digital Input Reading

The 60 inputs are grouped as seven sets of eight inputs, and one set of four inputs. Each group of inputs is accessed through an I/O memory address, which is an offset from the base decode address. Inputs are grouped as follows:

Group 1: Inputs DI1 to DI8	I/O address = Base Address
Group 2: Inputs DI9 to DI16	I/O address = Base Address + 1
Group 3: Inputs DI17 to DI24	I/O address = Base Address + 2
Group 4: Inputs DI25 to DI32	I/O address = Base Address + 3
Group 5: Inputs DI33 to DI40	I/O address = Base Address + 4
Group 6: Inputs DI41 to DI48	I/O address = Base Address + 5
Group 7: Inputs DI49 to DI56	I/O address = Base Address + 6
Group 8: Inputs DI57 to DI60	I/O address = Base Address + 7

Input	Offset from Base Address	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Group 1	0	Input8	Input7	Input6	Input5	Input4	Input35	Input2	Input1
Group 2	1	Input16	Input15	Input14	Input13	Input12	Input11	Input10	Input9
Group 3	2	Input24	Input23	Input22	Input21	Input20	Input19	Input18	Input17
Group 4	3	Input32	Input31	Input30	Input29	Input28	Input27	Input26	Input25
Group 5	4	Input40	Input39	Input38	Input37	Input36	Input35	Input34	Input33
Group 6	5	Input48	Input47	Input46	Input45	Input44	Input43	Input42	Input41
Group 7	6	Input56	Input55	Input54	Input53	Input52	Input51	Input50	Input49
Group 8	7	Not used				Input60	Input59	Input58	Input57

CHAPTER 1 CONFIGURATION

1.1 Register map

Configuration of the IO104-60IN is accomplished via two registers in the I/O map: Base Address + 0x00 and 0x07

Base Address Offset	Function
0x00	Base address/Input 1-8
0x01	Input 9-16
0x02	Input 17-24
0x03	Input 25-32
0x04	Input 33-40
0x05	Input 41-48
0x06	Input 49-56
0x07	Write flag + Input 57-60

Table 9: Register map

1.2 Configuration/DIN base address

The IO104-60IN can place the I/O block on any 8-byte boundary. When setting a base address, the value to write to the base address register is bits 9-3 of the desired base address. The address register is usually hidden, and in its place are inputs 1-8. To access the register, the write-lock must be enabled

For example:

To move the IO104-60IN base address to 0x240, write 0x48 to the base address register.

To move the IO104-60IN base address to 0x260, write 0x4C to the base address register.

Offset: 0x00

Bit	7	6	5	4	3	2	1	0
Function	Resv'd	ADDR 9	ADDR 8	ADDR 7	ADDR6	ADDR5	ADDR4	ADDR3

Table 10: Configuration/DIO base address

1.3 Write Lock

Offset: 0x07

Bit	7	6	5	4	3	2	1	0
Function	WREN	0	0	0	DI60	DI59	DI58	DI57

Table 18: Write Lock register

WREN signals whether the configuration register at Base Address + 0x00 is accessible. A
 1: 0x00 contains the base address,
 0: 0x00 contains DI1-DI8

To enable changes to the board configuration, the Key sequence must be written to the Write Lock register.

The key sequence to unlock the board configuration is: **0xAA → 0x55 → 0x5A → 0xA5**

When the configuration is unlocked, WREN will be 1.

Any write to this register, which does not follow this sequence will reset the sequence. Once the board configuration is unlocked, writing any new value to the Write Lock Register will lock the board configuration. Writing 0xFF to the Write Lock register while configuration is unlocked will both save the current configuration to the on board EEPROM and lock the board configuration. Changes to the Base Address do not take effect until the configuration is written to the EEPROM.

1.4 Recovery

If the address of the IO104-60IN is not know, it can be recovered through the use of writes to address 0x300. Writing the key sequence to address 0x300 will temporarily set the IO104-60IN base address to 0x300. At this point, the write lock can be used to enable configuration.

The recovery sequence is: **0xAA → 0x55 → 0x5A → 0xA5**

If there is one incorrect write, the sequence must start again from the beginning.

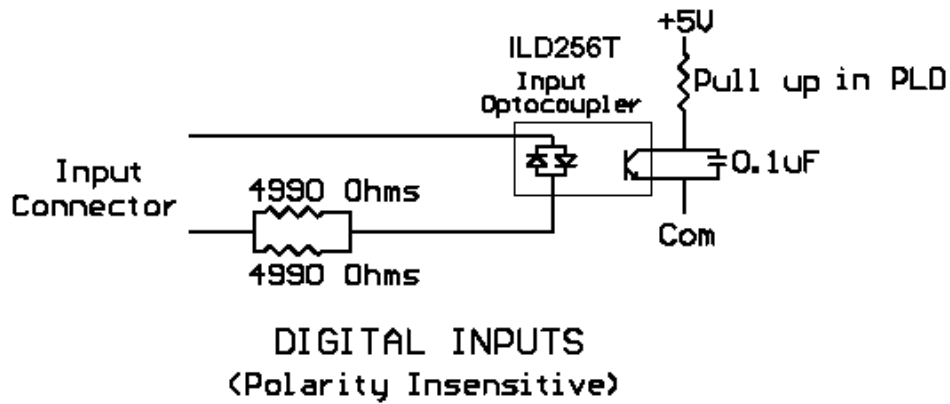
Initiating a recovery in a system with more that one IO104-60IN will cause all IO104-60IN boards to occupy the same base address.

The IO104-60IN base address will remain at the recovery address until the configuration is written to the EEPROM.

1.5

Input Series Resistor and Opto-Coupler

Each input has two 4990 ohm resistors in parallel with each other and in series with the bi-directional input opto-coupler as shown.



IO104-60IN Input Locations

