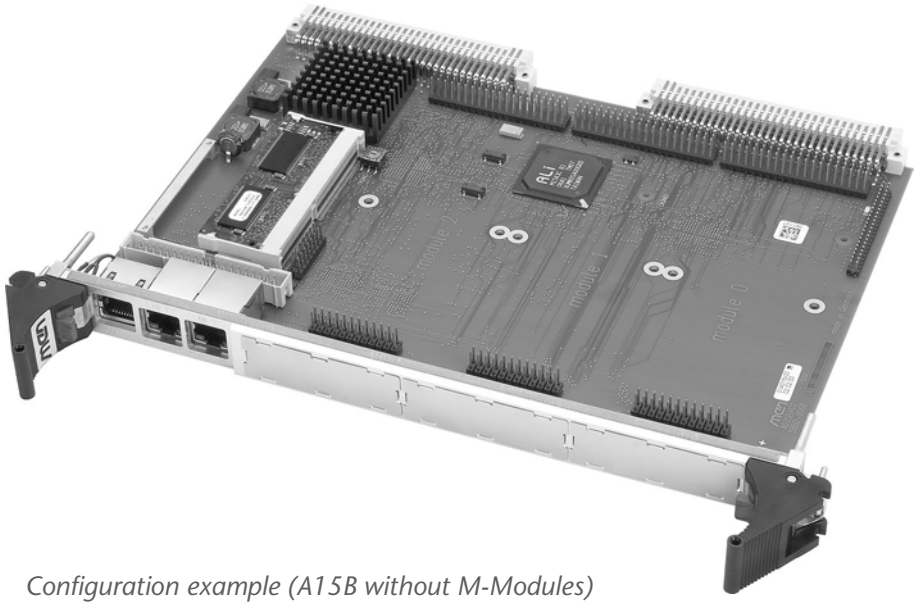
Embedded Solutions

A15 – 6U VME64 MPC8245 SBC with Mezzanines



Configuration example (A15B without M-Modules)

User Manual

mikro elektronik
gmbh · nürnberg

A15 – 6U VME64 MPC8245 CPU Board with Mezzanines

The A15 is a PowerPC® MPC8245 based single-board computer for embedded applications. It features full VME64 support and it can be used as a master or a slave in a VMEbus environment. The A15 provides 1 MB local dual-ported SRAM for slave access and communication between the local CPU and another VMEbus master.

The CPU card comes with the MPC8245 PowerPC® with 400 MHz clock frequency and local 32-bit/33-MHz PCI data bus. It is a complete state-of-the-art SBC offering DRAM, Flash and CompactFlash® memory, dual Fast Ethernet, four COMs, USB, IDE and keyboard/mouse interfaces as well as an optional onboard hard disk. A software-loadable FPGA is available with A15B for individual user-defined functions such as additional UARTs, a CAN bus interface, DSP functions etc.

Depending on the kind of I/O requirements, various standard versions of A15 are availabe for different mezzanine standards.

The A15 can be equipped with PMC or M-Module™ mezzanine cards supporting both front I/O and rear I/O. PMCs may particularly be used for intelligent telecom I/O, while M-Modules™ are recommended for real-world I/O like analog/binary process I/O and instrumentation I/O. The modular combination of I/O functionality on a single-board computer allows to build up tailored control systems which appear as customized solutions based on standard components.

The A15 comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

The A15 single-board computer is partly compatible with the MVME2100 board by Motorola.

Technical Data

CPU

- PowerPC®
  - MPC8245
  - 400 MHz
  - Double precision FPU

Memory

- L1 Cache integrated in MPC8245
- Up to 512 MB SDRAM system memory
  - One 144-pin SO-DIMM slot for SDRAM modules
  - 133 MHz memory bus frequency

  For more information on available standard versions see online data sheets:
  - A15B
  - A15C
- 2 MB Boot Flash
- 32 MB application Flash (optional)
  - 64-bit data bus
- Serial EEPROM 4 kbits for factory settings
- CompactFlash® card interface
  - Via onboard IDE
  - Type I
  - True IDE

Mass Storage

- Parallel IDE (PATA)
  - One port for local CompactFlash®
  - One port for local hard-disk drive
  - Drive can be connected via ribbon cable or mounted directly on the CPU board using MEN adapter kit
  - Only one VMEbus slot needed even with hard disk
  - IDE port also available for rear I/O, alternatively to onboard connector

I/O

- USB
  - One USB 1.1 port
  - Accessible via I/O connector J2
  - OHCI implementation
  - Data rates up to 12 Mbit/s
  - External PHY
- Ethernet
  - Two 10/100Base-T Ethernet channels
  - RJ45 connectors with two LEDs at front panel

- One RS232 UART (COM1)
  - RJ45 connector at front panel
  - Data rates up to 115.2 kbit/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS; DCD, DSR, DTR
  - 16550 compliant
- A15C: One RS232 UART (COM2)
  - RJ45 connector at front panel
  - Data rates up to 115.2 kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS; DCD, DSR, DTR
  - 16550 compliant
- A15B: One UART (COM2)
  - Accessible via I/O connector
  - Physical interface at front panel or using SA-Adapter™ via 10-pin ribbon cable on I/O connector, depending on board version
  - RS232..RS485, isolated or not: for free use in system (e.g., cable to front)
  - Data rates up to 115.2 kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: full support; lines depend on SA-Adapters™
  - 16550 compliant
- Two UARTs (COM3/COM4)
  - Accessible via I/O connector
  - Data rates up to 115.2 kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: none
  - 16550 compliant
- PS/2 keyboard/mouse
  - Accessible via I/O connector
  - Requires external PHY

Rear I/O

- A15C:
  - PMC 0
- A15B:
  - IDE (alternatively to onboard connector)
  - GPIO (alternatively to onboard connector)
  - M-Module™ 0, 1 and 2

Mezzanine Extensions

- A15C: Two PMC slots
  - Compliant with PMC standard IEEE 1386.1
  - Up to 64-bit/64-MHz, 3.3 V V(I/O)
  - PMC I/O module (PIM) support through J4 (slot 0)
- A15B: Three M-Module™ slots
  - Compliant with M-Module™ standard
  - Characteristics: A08, A24, D16, D32, INTA, INTC

Miscellaneous

- Serial real-time clock with integrated 56-byte NVRAM
- Serial hardware watchdog in supervisory circuit
- Temperature sensor
- Hex switch for user settings
- User LEDs (integrated into COM1 connector)
- Reset button in ejector handle
- Abort button via I/O connector
- JTAG/BDM connector

Local PCI Bus

- 32-bit/33-MHz, 3.3 V V(I/O)
- Compliant with PCI Specification 2.2

VMEbus

- Compliant with VME64 Specification
- Slot-1 function with auto-detection
- Master
  - D08(EO):D16:D32:D64:A16:A24:A32:ADO:BLT:RMW
- Slave
  - D08(EO):D16:D32:D64:A16:A24:A32:BLT:RMW
- 1 MB shared fast SRAM
- DMA
- Mailbox functionality
- Interrupter D08(O):I(7-1):ROAK
- Interrupt handler D08(O):IH(7-1)
- Single level 3 fair requester
- Single level 3 arbiter
- Bus timer
- Location Monitor
- Performance
  - Coupled read/write D32 non-block transfer rate 6.5 MB/s
  - DMA read/write D32 BLT transfer rate 12.1 MB/s
  - DMA read/write D64 MBLT transfer rate 25 MB/s

Electrical Specifications

- Supply voltage/power consumption:
  - +5 V (-3%/+5%), 1.3 A typ.
  - ±12 V (-5%/+5%), only used for mezzanines, tbd.
- MTBF: 126 000 h @ 40°C (derived from MIL-HDBK-217F)

Mechanical Specifications

- Dimensions: standard double Eurocard, 233.3 mm x 160 mm
- Weight (without mezzanines and accessories): 330 g

Environmental Specifications

- Temperature range (operation):
  - 0..+60°C or -25..+85°C
  - Airflow: min. 10 m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300 m to +3000 m
- Shock: 15 g, 11 ms
- Bump: 10 g, 16 ms
- Vibration (sinusoidal): 2 g, 10..150 Hz
- Conformal coating on request

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst) with regard to CE conformity

BIOS

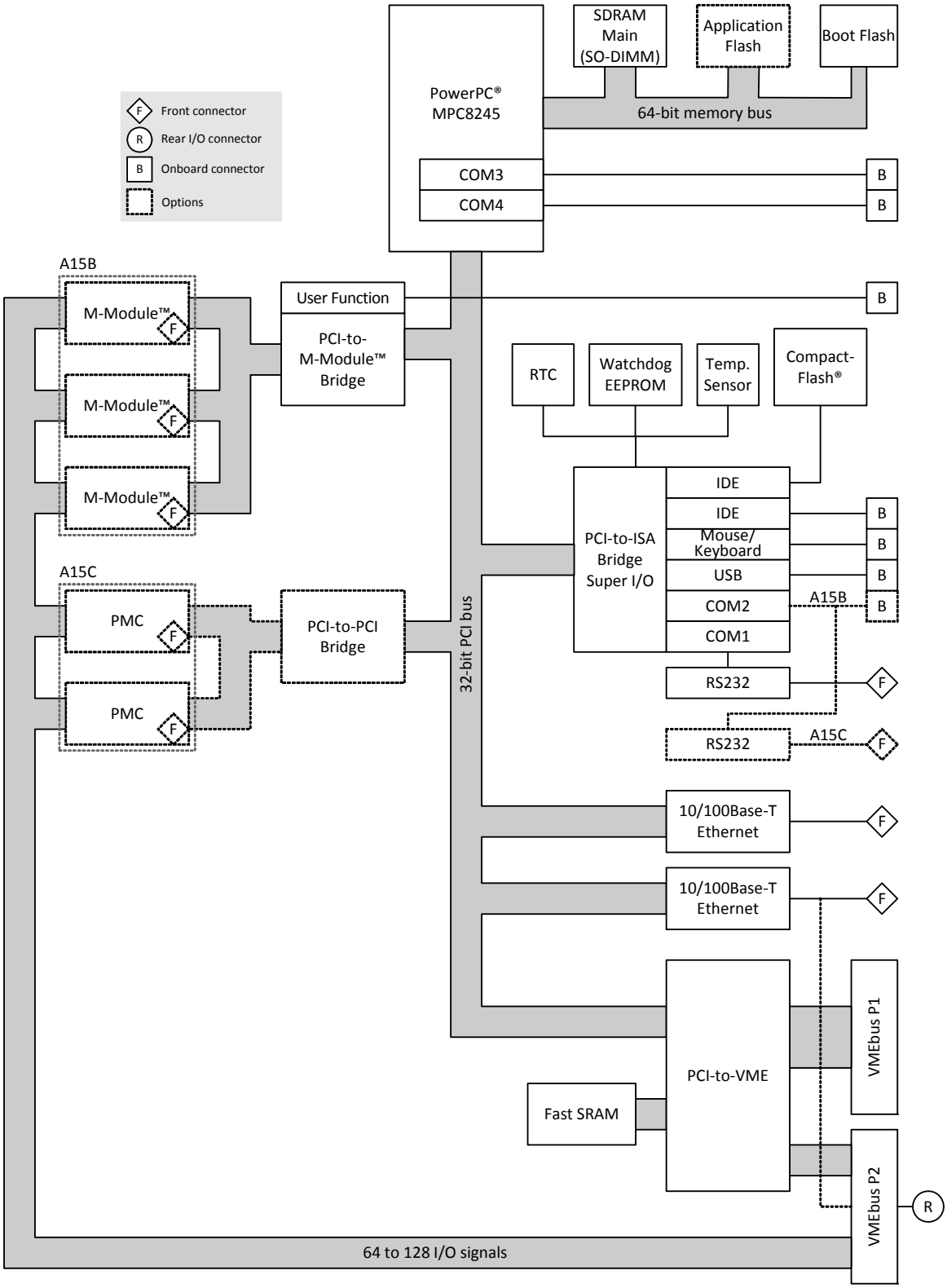
- MENMON™

Software Support

- Linux
- VxWorks®
- OS-9®
- QNX®
- For more information on supported operating system versions and drivers see online data sheets:
  - A15B
  - A15C

See also Configuration Options.

Block Diagram



Configuration Options

CPU

- MPC8245, 400 MHz

Memory

- System RAM
  - 128 MB, 256 MB or 512 MB
- CompactFlash®
  - 0 MB up to maximum available
- Boot Flash
  - 2 MB
- Application Flash
  - 32 MB, 64-bit data bus

Mezzanine Slots

- 2 PMC
- 3 M-Modules™

Operating Temperature

- 0..+60°C
- -20..+85°C

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

For available standard configurations see online data sheets:

- A15B
- A15C

Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Issue	Comments	Date
E1	First issue	2003-07-10
E2	Second issue	2004-01-13
E3	Third issue	2004-02-06
E4	Update of VMEbus chapter	2006-05-05
E5	General update, errors corrected; PC-MIP removed; note on VMEbus *STDBY*; corrections for MENMON 2nd edition	2008-09-01
E6	General update	2012-03-15
E7	All product versions now delivered with DRAM installed; general improvements	2012-11-29

Conventions

This sign marks important notes or warnings concerning the use of voltages which can lead to serious damage to your health and also cause damage or destruction of the component.

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

comment — Comments embedded into coding examples are shown in green color.

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ#
/IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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RoHS

Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.

WEEE Application

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.

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Contents

Figures

Tables

1 Getting Started

This chapter will give an overview of the board and some hints for first installation in a system as a "check list".

1.1 Maps of the Board

Figure 1. *General board map – top view*

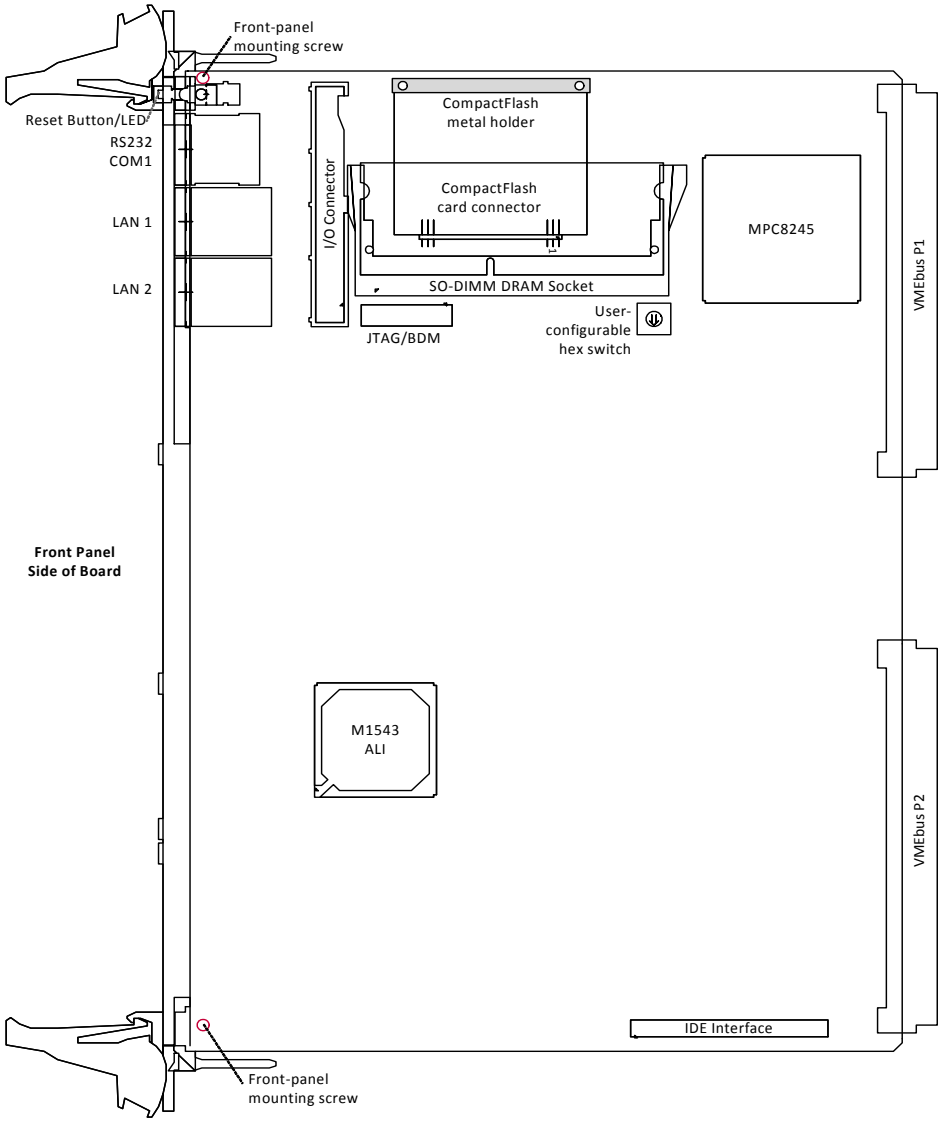


Figure 2. *A15B board map – CPU board with M-Modules – top view*

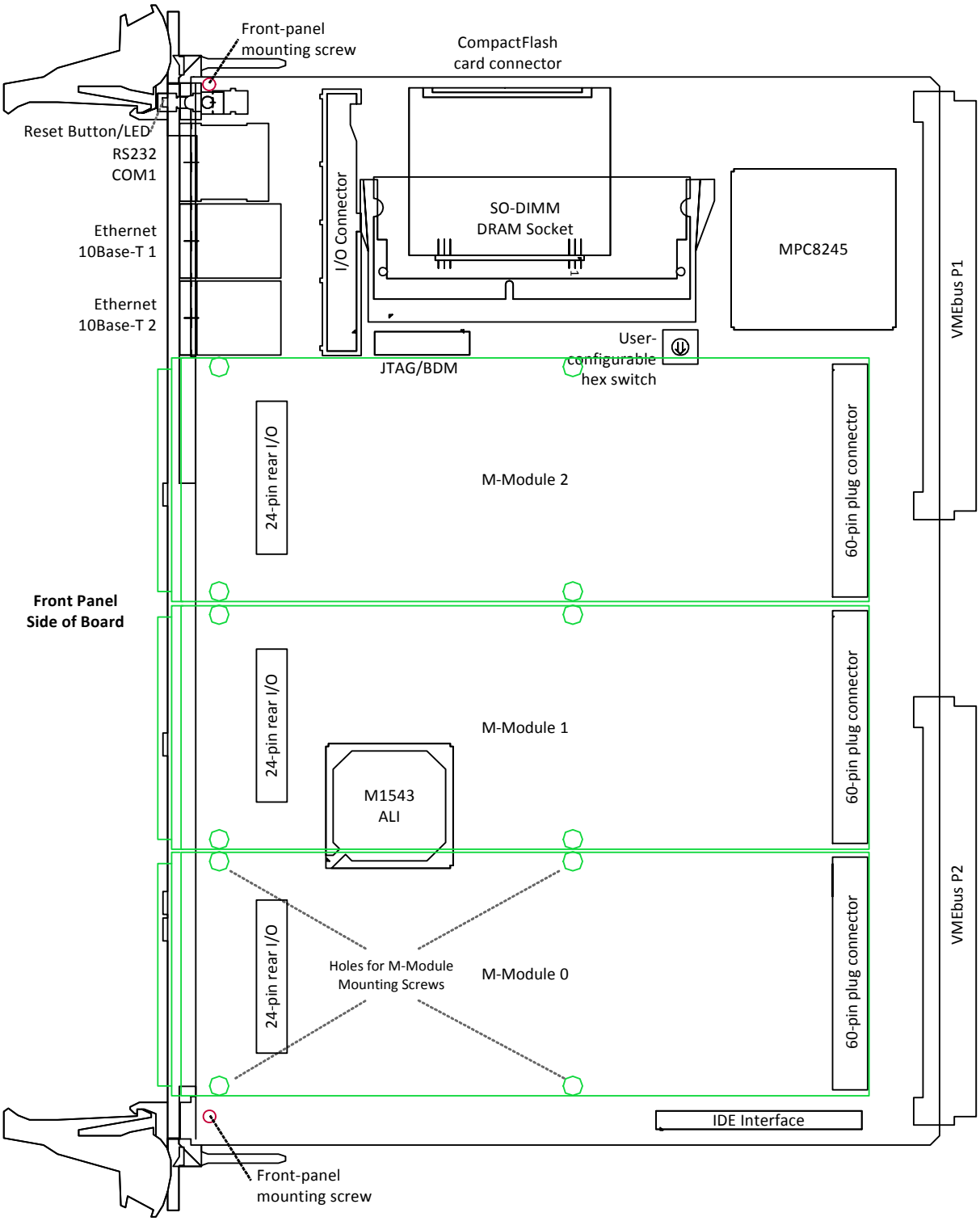
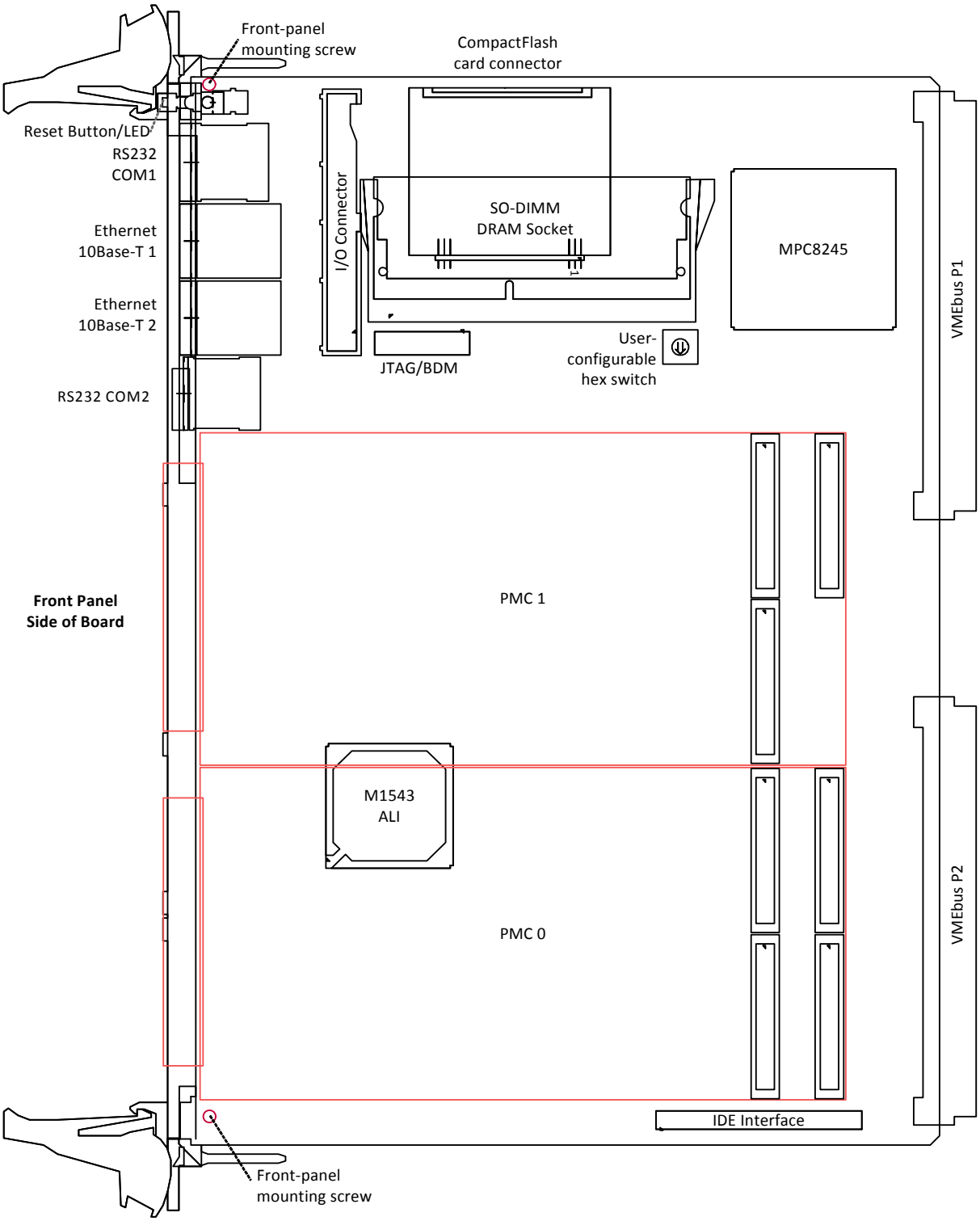


Figure 3. *A15C board map – CPU board with PMCs and COM2 at front – top view*



1.2 Configuring the Hardware

You should check your hardware requirements before installing the board in a system, since most modifications are difficult or even impossible to do when the board is mounted in an enclosure.

The following check list will give an overview on what you might want to configure.

☑ CompactFlash

Refer to Chapter 2.5.3 CompactFlash on page 29 for a detailed installation description and hints on supported CompactFlash cards.

☑ M-Modules

Refer to Chapter 2.6.3 Installing an M-Module Mezzanine Module on page 33 for a detailed installation description.

☑ PMC modules

Refer to Chapter 2.7.1 Installing a PMC Mezzanine Module on page 35 for a detailed installation description.

☑ Serial interface adapter (SA-Adapter) (only A15B)

You can install a standard serial interface such as RS232 on COM2 using MEN SA-Adapters on the A15B's I/O connector.

Refer to Chapter 2.10 I/O Expansion Connector on page 42 and Chapter 2.11 Serial Ports COM1/COM2 on page 45 for detailed installation descriptions.

1.3 Integrating the Board into a System

The A15 is a complex board and setting it up requires experience. You can use the following check list when installing the CPU board in a system for the first time and with minimum configuration.

The board is completely trimmed on delivery. Perform the following procedure **without any mezzanine module installed**!

- ☑ Power-down the system.
- ☑ Remove all boards from the VMEbus system.
- ☑ Insert the A15 into slot 1 of the system, making sure that the connectors are properly aligned.
- ☑ Connect a terminal to the standard RS232 interface COM1 (RJ45 connector).
- ☑ Set your terminal to the following protocol:
  - 9600 baud data transmission rate
  - 8 data bits
  - 1 stop bit
  - No parity
- ☑ Power-up the system.
- ☑ The terminal displays a message similar to the following:

```
 ____________________ Secondary MENMON for MEN A015 2.1 ____________________________
|                                                                                   |
|          (c) 2002 - 2005 MEN Mikro Elektronik GmbH Nuremberg                     |
|         MENMON 2nd Edition, Created  Jul 17 2006     08:08:21                    |
|___________________________________________________________________________________|
|      CPU Board: A015a00             |            CPU: MPC8245                     |
|  Serial Number: 422                 |  CPU/MEM Clock: 400 / 132 MHz               |
|    HW Revision: 02.05.00            |    DIMM Module: 128 MB 333                  |
\___________________________________________________________________________________/
Setting speed of NETIF 0 to AUTO
Setting speed of NETIF 1 to AUTO

press 'ESC' for MENMON, 's' for setup
Test SDRAM                    : OK
Test ETHER0                   : OK
Test ETHER1                   : OK
Test EEPROM                   : OK
Test RTC                      : OK
Test LM75                     : OK
(Can't load BOOTLOGO.BMP)

NOW AUTOEXECUTING: BO
No default start address configured. Stop.
Setup network interface CLUN 0x02, 00:c0:3a:29:01:a6 AUTO
 Telnet daemon started on port 23
 HTTP daemon started on port 80
MenMon>
```

- ☑ Now you can use the MENMON debugger (see detailed description in Chapter 3 MENMON on page 80).
- ☑ Observe the installation instructions for the respective software.

1.4 Installing Operating System Software

The board supports VxWorks, Linux, OS-9 and QNX.

By default, no operating system is installed on the board. Please refer to the respective manufacturer's documentation on how to configure your operating system image!

You can find any software available in the A15B and A15C pages on MEN's website.

1.5 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPUs. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned (Chapter 5.1 Literature and Web Resources on page 110).

Please note that the board BSPs for the different operating systems may not support all the functions of the A15. For more information on hardware support please see the respective BSP data sheet on MEN's website:

- A15B
- A15C

2.1 Power Supply

The board is supplied with +5 V and ±12 V via the VMEbus. However, ±12 V may be required only by some mezzanine modules.

The onboard power supply generates the 2.1 V core voltage and 3.3 V I/O voltage of the PowerPC.

2.2 Clock Supply

The clock supply generates all clocks for the onboard devices (PowerPC, SDRAM, host bridge, PCI bus devices). The clock frequency is factory-set.

The local PCI clock operates at 33 MHz.

2.3 PowerPC CPU

The board is equipped with the MPC8245 Kahlua II processor, which includes a 32-bit superscalar PowerPC 603e core, the integrated host-to-PCI bridge, and two UARTs.

2.3.1 General

The PowerPC architecture, developed jointly by Motorola, IBM, and Apple Computer, is based on the POWER architecture implemented by the RS/6000™ family of computers. The PowerPC architecture takes advantage of recent technological advances in such areas as process technology, compiler design, and RISC microprocessor design to provide software compatibility across a diverse family of implementations, primarily single-chip microprocessors, intended for a wide range of systems.

2.3.2 Heat Sink

A heat sink is provided to meet thermal requirements.

2.4 Bus Structure

2.4.1 Host-to-PCI Bridge

The integrated host-to-PCI bridge (internal in MPC8245) is used as host bridge and memory controller for the PowerPC processor. All transactions of the PowerPC to the PCI bus are controlled by the host bridge. The SDRAM and boot Flash are connected to the local memory bus of the integrated host-to-PCI bridge.

The PCI interface is PCI bus Rev. 2.2 compliant and supports all bus commands and transactions. Master and target operations are possible. Only big-endian operation is supported.

2.4.2 Local PCI Bus

The local PCI bus is controlled by the integrated host-to-PCI bridge. It runs at 33 MHz. The I/O voltage is fixed to 3.3 V. The data width is 32 bits.

Major functional elements of the board, such as Ethernet, are connected to the local PCI bus.

2.4.3 PCI-to-ISA Bridge Super I/O Controller

The M1543 provides integrated Super I/O (2 serial ports), system peripherals (ISP) (2 82C59 and serial interrupt, 1 82C54), advanced features (type F and distributed DMA) in the DMA controller (2 82C37), PS2 keyboard/mouse controller, 2-channel dedicated IDE master controller with Ultra-33 specification and System Management Bus (SMB).

M1543 also provides a PCI-to-ISA IRQ routing table, and level-to-edge trigger transfer.

2.4.4 PCI-to-VMEbus Bridge

The board has a PCI-to-VME bridge for connection to the VMEbus. It is implemented in an FPGA. On the local PCI bus this bridge is a master. The local processor can thus freely access the VMEbus (master). For communication in multiprocess applications, the bridge has a fast communication memory of 1MB size. This memory can be accessed both from the local processor and from the VMEbus (slave).

2.4.5 PCI-to-PCI Bridge

The A15C board has a secondary PCI bus for accesses to PMC modules. It is controlled by an HB2 PCI-to-PCI bridge from Hint/PLX.

2.5 Memory

2.5.1 SDRAM

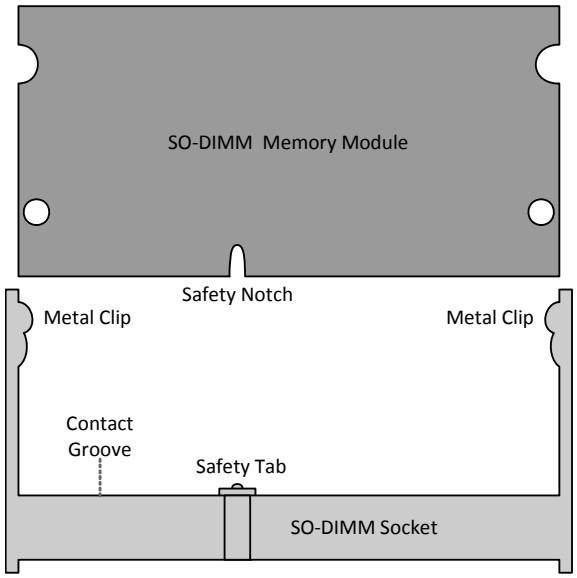
One SDRAM bank (bank 0) is implemented on the board. Bank 0 is connected to a 144-pin SO-DIMM connector. The current board version supports SO-DIMMs up to 512 MB.

Note: A15 boards with MENMON versions lower than 2.1 support only up to 256 MB DRAM. MENMON 2nd edition, starting from MENMON version 2.1, supports up to 512 MB DRAM.

The board is shipped with a **tested DRAM SO-DIMM module installed**. If for any reason you need to exchange or install an SO-DIMM module, please stick to the following procedure.

Note: MEN gives no warranty on functionality and reliability of the board if you use any other module than that qualified and/or supplied by MEN. Please contact either MEN directly or your local MEN sales office.

Figure 4. *SO-DIMM DRAM installation*



The DRAM module will only fit as shown above because of a safety tab on the SO-DIMM socket which requires a notch in the SO-DIMM module.

- ☑ Power down the system before installing a SO-DIMM module to avoid damage of the board!
- ☑ Place the memory module into the socket at a 45° angle and make sure that the safety tab and notch are aligned.
- ☑ Carefully push the memory module into the contact groove of the socket.
- ☑ Press the memory module down until it clicks into place.
- ☑ The metal clips of the socket now hold the memory module in place.
- ☑ To release the module, squeeze both metal clips outwards and carefully pull the module out of the socket.

2.5.2 Flash

2.5.2.1 Boot Flash

The board has onboard Flash. It is controlled by the integrated host-to-PCI bridge of the MPC8245 and can accommodate 2 MB or 4 MB. The data bus is 8 bits wide.

Flash memory contains the boot software for the MENMON/operating system bootstrapper and application software. The MENMON sectors are software-protected against illegal write transactions through a password in the serial download function of MENMON (cf. Chapter 3.4 Updating Boot Flash and CompactFlash on page 84).

2.5.2.2 Application Flash

The board also has an optional 32 MB application Flash. The data bus is 64 bits wide. The Flash is controlled by chip select signal RCS3 of the MPC8245.

2.5.3 CompactFlash

CompactFlash is a standard for small form factor ATA Flash drives. It is electrically compatible to the PC Card 1995 and PC Card ATA standards.

The CompactFlash standard is supported by industry's leading vendors of Flash cards and others.

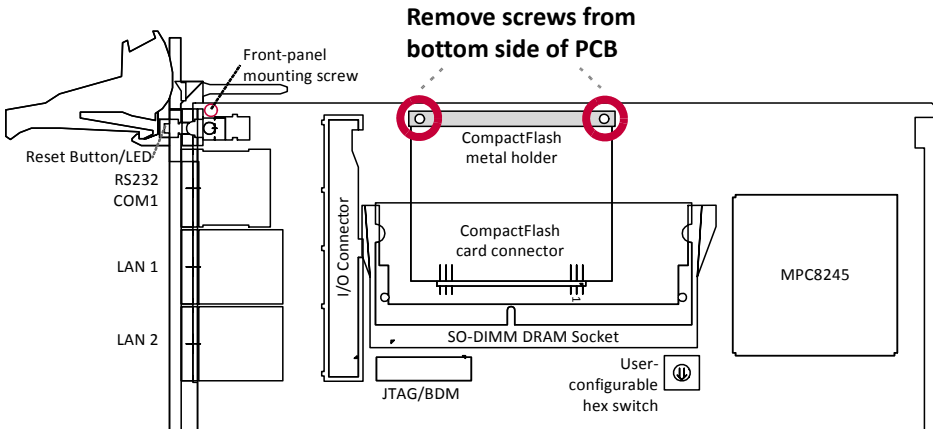
CompactFlash cards are operated in a True IDE Mode.

2.5.3.1 Installing a CompactFlash Card

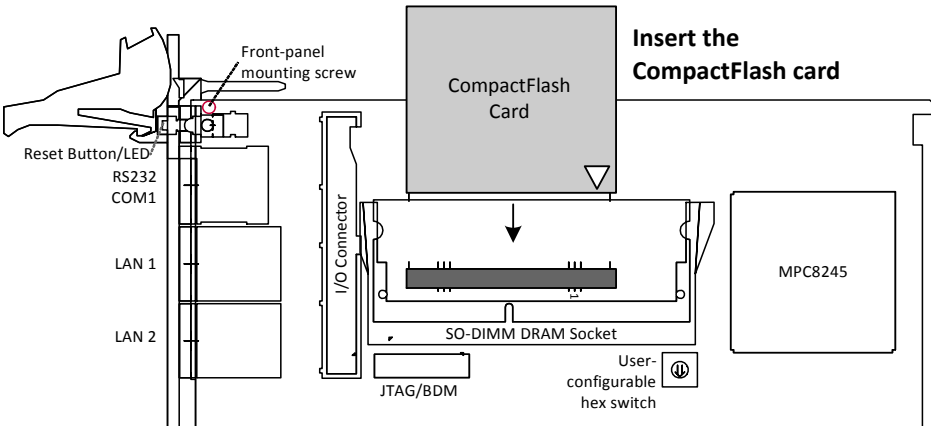
The CompactFlash slot is within the SO-DIMM DRAM socket, i.e. the CompactFlash card is placed below a DRAM module.

The board is shipped without a CompactFlash card installed. To install CompactFlash, please stick to the following procedure.

- ☑ Power down your system and remove the board from the system.
- ☑ Remove the SO-DIMM module installed in the DRAM socket as described in Chapter 2.5.1 SDRAM on page 28.
- ☑ Remove the metal holder that is included with the board to secure the Compact-Flash card. To do this, loosen and remove the two cross-recess screws from the bottom side of the PCB.



☑ Insert the CompactFlash card carefully as indicated by the arrow on top of the card, making sure that all the contacts are aligned properly and the card is firmly connected with the card connector.



☑ Reinstall the metal holder: Place the holder over the CompactFlash card and carefully align the screw holes of the holder and the board. Make sure to include the nut between each screw and the PCB.

☑ Reinstall your SO-DIMM module.

☑ To remove the CompactFlash card you must again remove and then reinstall the SO-DIMM module and metal holder as described above.

☑ Observe manufacturer notes on usage of CompactFlash cards.

2.5.3.2 Supported CompactFlash Cards

The board supports standard CompactFlash cards.

You can order suitable CompactFlash cards from MEN. Please see the A15B and A15C pages on MEN's website for ordering options.

2.5.4 EEPROM

The board has a 4-kbit serial EEPROM for factory data, MENMON parameters, and for the VxWorks bootline.

2.6 M-Module Slots (A15B)

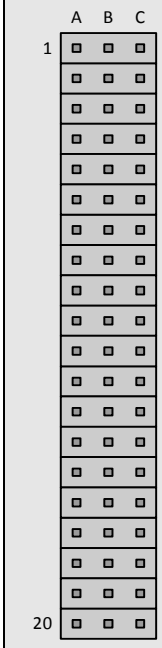
The M-Module slots enable the user to add a number of I/O functions to the CPU board. The wide range of standardized M-Modules includes not only process I/O modules but also interface extensions, network boards (such as Profibus, CAN bus etc.), DSP and transputer modules and special-purpose functions.

The A15 has three M-Module slots and supports the following M-Module characteristics: D16, D32, A08, A24, INTA, INTC.

2.6.1 Connection

The signals from the CPU board are fed to the M-Module via three 20-pin plug connector rows. These connectors correspond to connectors on the M-Module. The pin assignment corresponds to the M-Module specification (see Chapter 5.1 Literature and Web Resources on page 110).

Table 1. *Pin assignment of the 60-pin M-Module plug connectors*



	A	B	C
1	CS#	GND	AS#
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	-	D20
7	A06	-	D21
8	A07	GND	D22
9	D08/A16	D00/A08	-
10	D09/A17	D01/A09	-
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	DS1#	DS0#	D29
18	DTACK#	WRITE#	D30
19	IACK#	IRQ#	D31
20	RESET#	SYSCLK	DS2#

2.6.2 Addressing the M-Modules

The PowerPC can address M-Modules via the local PCI bus. The PCI-to-M-Module bridge is implemented in an FPGA. The three M-Modules are mapped within the PCI target as shown in the following table. The address determines the access mode in which the respective M-Module is addressed. The interrupt of each M-Module can be handled in the Control/Status Register. The interrupts of all M-Modules are summarized in the bridge as the PCI interrupt of this target device.

Table 2. *M-Module address map*

Base Address Register/ Block Size	Offset Address Range	Function
M-Module 0 32M	0x 0000 0000..0x 00FF FFFF	A24/D32 access
	0x 0100 0000..0x 01FF FCFF	A24/D16 access
	0x 01FF FD00..0x 01FF FDFF	A08/D32 access
	0x 01FF FE00..0x 01FF FEFF	A08/D16 access
	0x 01FF FF00..0x 01FF FF03	A08/D16 IACK
	0x 01FF FF04..0x 01FF FF07	Control/Status Register
M-Module 1 32M	0x 0200 0000..0x 02FF FFFF	A24/D32 access
	0x 0300 0000..0x 03FF FCFF	A24/D16 access
	0x 03FF FD00..0x 03FF FDFF	A08/D32 access
	0x 03FF FE00..0x 03FF FEFF	A08/D16 access
	0x 03FF FF00..0x 03FF FF03	A08/D16 IACK
	0x 03FF FF04..0x 03FF FF07	Control/Status Register
M-Module 2 32M	0x 0400 0000..0x 04FF FFFF	A24/D32 access
	0x 0500 0000..0x 05FF FCFF	A24/D16 access
	0x 05FF FD00..0x 05FF FDFF	A08/D32 access
	0x 05FF FE00..0x 05FF FEFF	A08/D16 access
	0x 05FF FF00..0x 05FF FF03	A08/D16 IACK
	0x 05FF FF04..0x 05FF EF07	Control/Status Register
	0x 0600 0000..0x 07FF FFFF	Reserved for FPGA user functions

M-Module Control/Status Register (0x*n*FFFF04) (read/write)

15..4	3	2	1	0
-	BE	PCI-RET	IEN	IRQ

BE Bus error

1 = Bus error occurred. Write 1 to clear.

PCIRET PCI retries

0 = PCI retries during access (slower)

1 = No PCI retries during access (faster) (default)

You should change this setting to 0 ("slower") if you can expect the M-Module access to be slower than 450 ns. Otherwise, leave the default setting as is.

IEN Interrupt enable bit

0 = Disable interrupt

1 = Enable interrupt

IRQ Interrupt pending

1 = Interrupt pending (reflects inverted *M_IRQ* line)

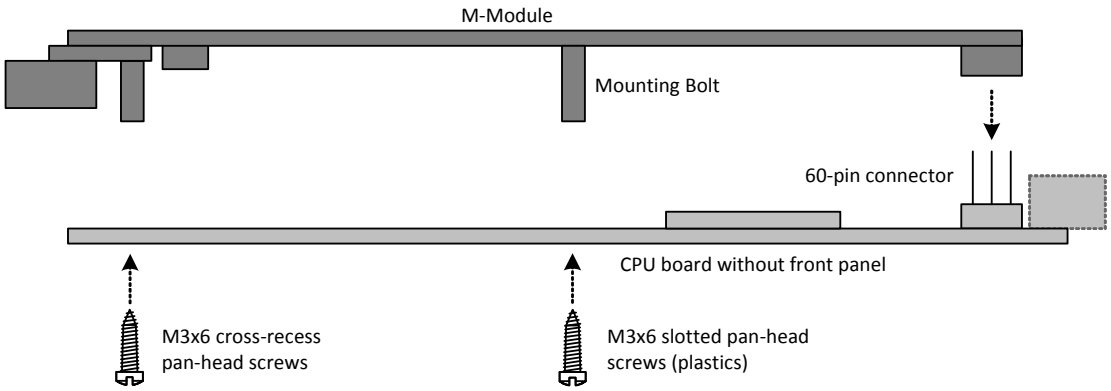
2.6.3 Installing an M-Module Mezzanine Module

Perform the following steps to install an M-Module:

- ☑ Power down your system and remove the CPU board from the system.
- ☑ Remove the filler panel from the board's front M-Module slot, if installed.
- ☑ Loosen the two front-panel mounting screws at the solder side of the CPU board and remove the whole front panel (see Figure 2, A15B board map – CPU board with M-Modules – top view, on page 21).
- ☑ Hold the M-Module over the target slot of the CPU board with the component sides facing each other.
- ☑ Align the 60-pin connectors of the M-Module and carrier board.
- ☑ Press the M-Module carefully but firmly onto the CPU board, making sure that the connectors are properly linked.
- ☑ Turn the CPU board upside down and use four M-Module mounting screws to fasten the M-Module on the solder side of the board.

You can order suitable mounting screws from MEN. Please see the A15B and A15C pages on MEN's website for ordering options.

Figure 5. *Installing an M-Module mezzanine module (A15B)*



2.7 PMC Slots (A15C)

The A15 board provides two PMC slots for extension such as graphics, Fast Ethernet, SCSI etc. The market offers lots of different PMC mezzanines.

The signaling voltage is set to 3.3 V, i. e. the CPU board has a 3.3-V voltage key (see Figure 6, Installing a PMC mezzanine module (A15C), on page 36) and can only carry PMC mezzanines that support this keying configuration. Mezzanine cards may be designed to accept either or both signaling voltages (3.3 V / 5 V).

The PMC slots support 32-bit and 64-bit PCI bus operation at 33 MHz or 66 MHz.

The connector layout is fully compatible to the IEEE1386 specification. For connector pinouts please refer to the specification (see Chapter 5.1 Literature and Web Resources on page 110).

Please note that only PMC slot 0 has a third 64-pin connector and therefore supports rear I/O connection. PMC slot 1 does not support rear I/O! See Table 25, Pin assignment of VMEbus rear I/O connector P2 – A15C – PMC on page 78.

Connector types:

- 64-pin, 1-mm pitch board-to-board receptacle according to IEEE 1386
- Mating connector:
  64-pin, 1-mm pitch board-to-board plug according to IEEE 1386

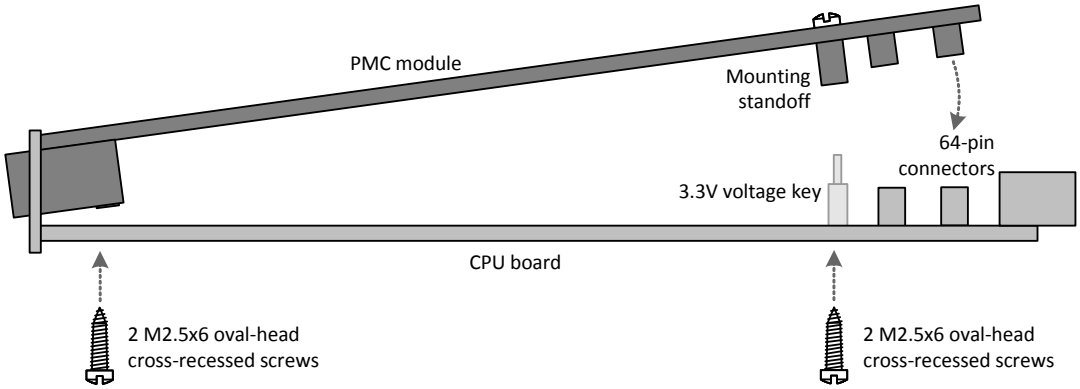
2.7.1 Installing a PMC Mezzanine Module

Perform the following steps to install a PMC module:

- ☑ Make sure that voltage keying of your PMC module matches the CPU board.
- ☑ Power down your system and remove the CPU board from the system.
- ☑ Remove the filler panel from the board's front PMC slot, if installed.
- ☑ The PMC module is plugged on the board with the component sides of the PCBs facing each other.
- ☑ Put the PMC module's front connector through the front slot at a 45° angle.
- ☑ Carefully put it down, making sure that the connectors are properly aligned.
- ☑ Press the PMC module firmly onto the board.
- ☑ Make sure that the EMC gasket around the PMC front panel is properly in its place.
- ☑ Screw the PMC module tightly to the CPU board at the bottom side of the PCB using four oval-head cross-recessed screws of type M2.5x6.

You can order suitable mounting screws from MEN. Please see the A15B and A15C pages on MEN's website for ordering options.

Figure 6. *Installing a PMC mezzanine module (A15C)*



2.8 IDE Interface

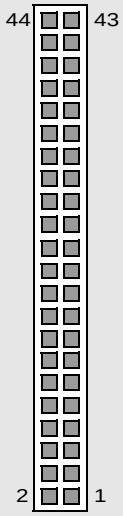
The board provides a 44-pin plug for IDE connection. The pinning of this connector is compliant with the ATA-4/ATAPI specification.

See Figure 1, General board map – top view, on page 20 for the position of the IDE connector.

Connector types:

- 44-pin, 2-row SMT plug, 2 mm pitch
- Mating connector:
  44-pin, 2-row IDC receptacle, 2 mm pitch

Table 3. *Pin assignment of the 44-pin IDE connector*



	44	GND	43	GND
	42	+5V	41	+5V
	40	GND	39	IDE_RACT#
	38	IDE_RCS3#	37	IDE_RCS1#
	36	IDE_RA[2]	35	IDE_RA[0]
	34	-	33	IDE_RA[1]
	32	-	31	IDE_RIRQ
	30	GND	29	IDE_RDAK#
	28	GND	27	IDE_RRDY
	26	GND	25	IDE_RRD#
	24	GND	23	IDE_RWR#
	22	GND	21	IDE_RDRQ
	20	-	19	GND
	18	IDE_RD[15]	17	IDE_RD[0]
	16	IDE_RD[14]	15	IDE_RD[1]
	14	IDE_RD[13]	13	IDE_RD[2]
	12	IDE_RD[12]	11	IDE_RD[3]
	10	IDE_RD[11]	9	IDE_RD[4]
	8	IDE_RD[10]	7	IDE_RD[5]
	6	IDE_RD[9]	5	IDE_RD[6]
	4	IDE_RD[8]	3	IDE_RD[7]
	2	GND	1	IDE_RRST#

Table 4. *Signal mnemonics for the IDE connector*

Signal	Direction	Function
+5V	-	+5V power supply, current-limited to 3A by a fuse
GND	-	Digital ground
IDE_RA[2:0]	out	IDE address [2:0]
IDE_RACT#	in	IDE active
IDE_RCS1#	out	IDE chip select 1
IDE_RCS3#	out	IDE chip select 3
IDE_RD[15:0]	in/out	IDE data [15:0]
IDE_RDAK#	out	IDE DMA acknowledge
IDE_RDRQ	in	IDE DMA request
IDE_RIRQ	in	IDE interrupt request
IDE_RRD#	out	IDE read strobe
IDE_RRDY	in	IDE ready
IDE_RRST#	out	IDE reset
IDE_RWR#	out	IDE write strobe

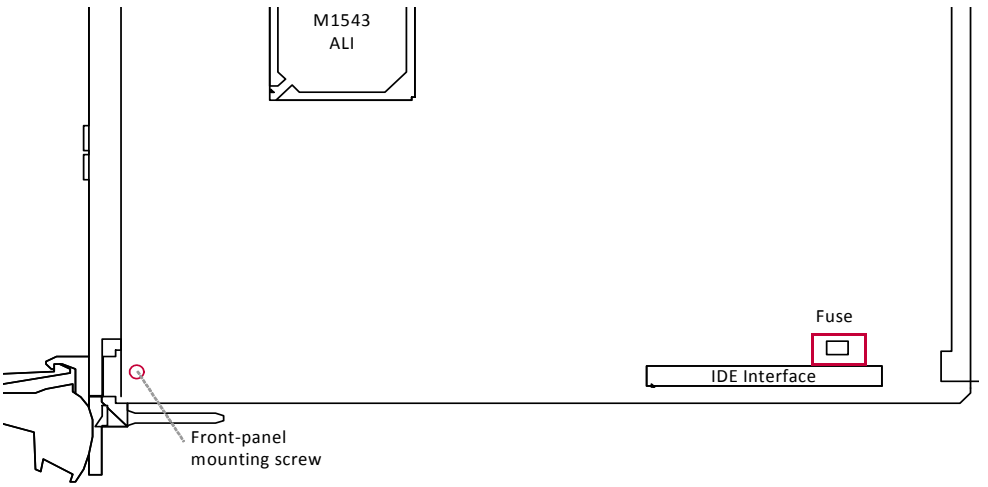
2.8.1 Fuse Protection

The IDE power supply is protected by a fuse. **This fuse is not intended to be exchanged by the customer. Your warranty for the A15 will cease if you exchange the fuse on your own.** Please send your board to MEN for repair if a fuse blows.

- Current rating: 3A
- Type: fast
- Size: 1206
- MEN part number: 5675-0003

The fuse is located on the top side of A15.

Figure 7. *Position of fuse for IDE power supply protection*



2.8.2 Installing a Hard Disk

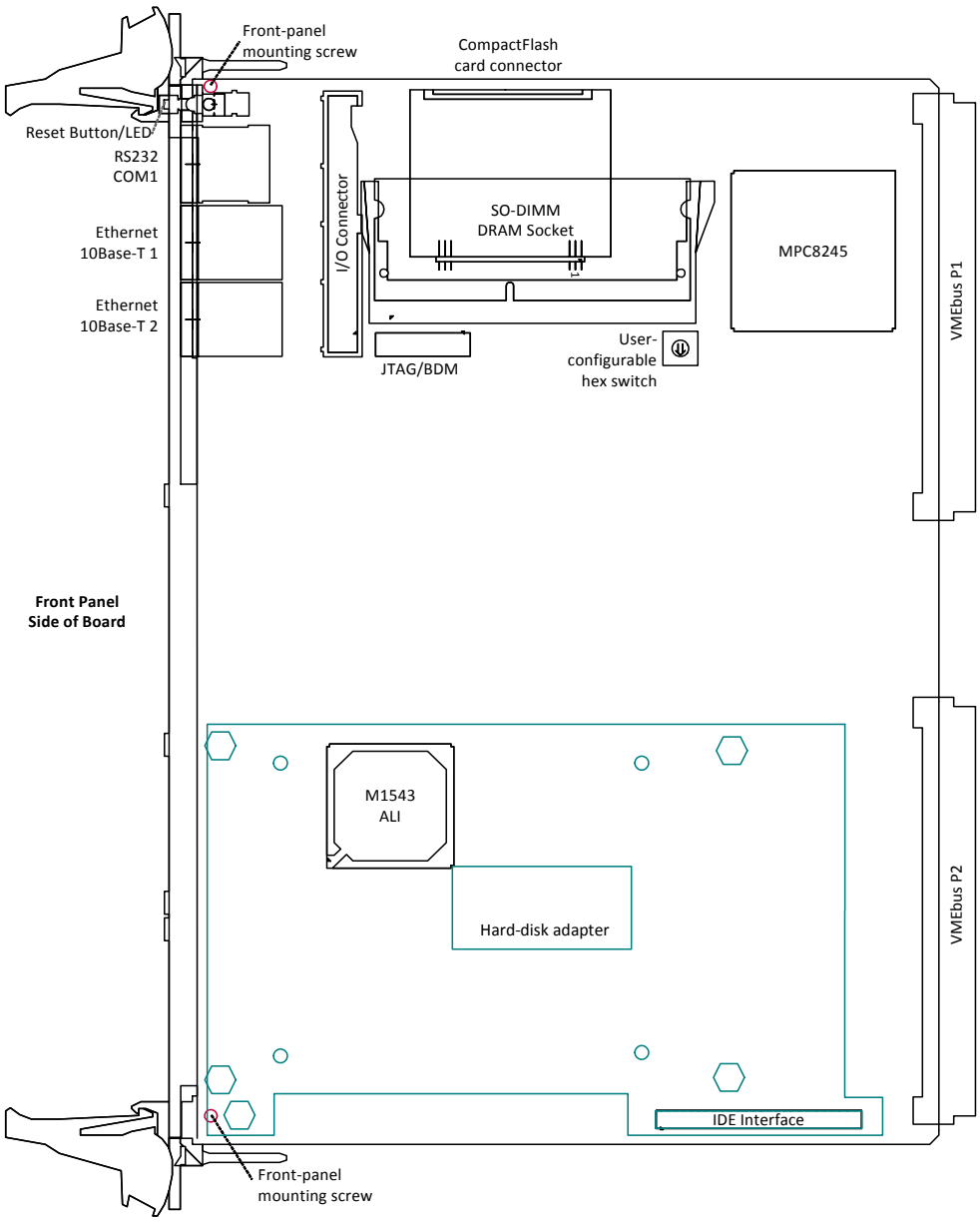
A hard-disk adapter card for installation of a 2.5", 9.5mm hard-disk drive is available from MEN. The adapter is designed in such a way that standard hard disks can easily be installed. For flexibility the adapter does not include the hard disk itself but includes all necessary screws to mount a standard hard disk.

Please see the A15B and A15C pages on MEN's website for ordering options.

If you want to install a hard disk on the board using MEN's adapter card, please keep in mind that the assembly occupies some of the space usually used for mezzanine modules. See Chapter 1.1 Maps of the Board on page 20 and Figure 8, Position of hard-disk adapter card on the board, on page 40.

The board needs only one slot in the system even with a hard disk installed. In this case no component pins of neighboring boards may exceed the interboard separation plane.

Figure 8. *Position of hard-disk adapter card on the board*



2.9 Ethernet Interface

The two Ethernet interfaces of the A15 support 10 Mbit/s and 100 Mbit/s as well as full-duplex operation and autonegotiation.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The MAC addresses on A15 are:

- LAN0: `0x 00 C0 3A 29 xx xx`
- LAN1: `0x 00 C0 3A 2A xx xx`

where "00 C0 3A" is the MEN vendor code, "29" and "2A" are the MEN product codes, and "xx xx" is the hexadecimal serial number of the product, which depends on your board, e. g. "... `00 2A`" for serial number "000042". (See Chapter 5.2 Finding out the Board's Article Number, Revision and Serial Number on page 112.)

2.9.1 Connection

Two standard RJ45 connectors with status LEDs are available at the front panel for connection to 10Base-T or 100Base-TX network environments. It is not necessary to switch between the two configurations!

The pin assignment corresponds to the Ethernet specification IEEE 802.3.

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

Table 5. *Pin assignment and status LEDs of the 8-pin RJ45 Ethernet 10Base-T/ 100Base-T connectors*

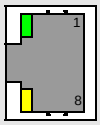
Lights up whenever there is transmit or receive activity	ACT		1	TX+
			2	TX-
			3	RX+
			4	Shield_R
			5	Shield_R
Lights up as soon as the link is established (10Base-T or 100Base-T)	LNK		6	RX-
			7	Shield_R
			8	Shield_R

Table 6. *Signal mnemonics of the Ethernet 10Base-T/100Base-T connectors*

Signal	Direction	Function
Shield_R	-	Shield via RC network
RX+/-	in	Differential pair of receive data lines
TX+/-	out	Differential pair of transmit data lines

2.10 I/O Expansion Connector

The board features a 40-pin I/O connector that implements several interfaces:

- Serial port COM2 (only A15B, compatible with MEN's SA-Adapters, see Chapter 2.11 Serial Ports COM1/COM2 on page 45)
- Serial ports COM3 and COM4 of the MPC8245
- Reset and abort button signals
- Two user-configurable LEDs (cf. Chapter 2.15 User LEDs on page 47)
- Keyboard/mouse (PS/2)
- USB 1.1 port

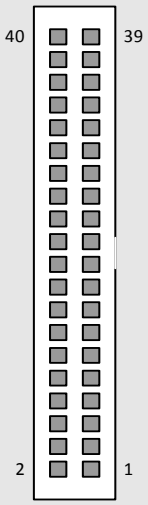
You can easily connect these interfaces using the AD67 I/O extension card from MEN, which plugs directly to the 40-pin connector, has convenient SA-Adapter slots and forms a 1-slot side card with additional front-panel connectors.

Please see the A15B and A15C pages on MEN's website for ordering options and the AD67 data sheet for more information.

Connector types:

- 40-pin low-profile plug, 2.54mm pitch, for ribbon-cable connection
- Mating connector:
  40-pin IDC receptacle, e.g. Elco Series 8290 IDC socket

Table 7. *Pin assignment of the 40-pin I/O expansion connector*



40	*Reserved*[1]	39	*Reserved*
38	*Reserved*	37	*Reserved*
36	*Reserved*	35	*Reserved*
34	*Reserved*	33	*Reserved*
32	RXD4	31	*Reserved*
30	TXD4	29	*Reserved*
28	RXD3	27	TXD3
26	+5V	25	GND
24	USBP0+	23	USBP0-
22	+5V	21	GND
20	MSDATA	19	MSCLK
18	KBDATA	17	KBCLK
16	LED2	15	LED1
14	ABRTBTN#	13	PWRBTN#
12	+5V	11	GND
10	RI2#	9	DCD2#
8	CTS2#	7	DSR2#
6	RTS2#	5	DTR2#
4	RXD2	3	TXD2
2	+5V	1	GND

[1] Reserved pins cannot be used but do not impair functionality.

Table 8. *Signal mnemonics of 40-pin I/O expansion connector*

	Signal	Direction	Function
Power	+5V	-	+5V power supply
	GND	-	Digital ground of respective interface
Mouse/ Key-board	KBDATA	out	Keyboard data
	KBCLK	out	Keyboard clock
	MSDATA	out	Mouse data
	MSCLK	out	Mouse clock
LEDs	LED1	out	LED1 cathode[1], can alternatively be used as a GPIO line
	LED2	out	LED2 cathode[1], can alternatively be used as a GPIO line
Button	ABRTBTN#	in	Abort button[2]
	PWRBTN#	in	Reset button[2]
M1543 COM2 (only A15B)	CTS2#	in	Serial port COM2 clear to send
	DCD2#	in	Serial port COM2 data carrier detect
	DSR2#	in	Serial port COM2 data set ready
	DTR2#	out	Serial port COM2 data terminal ready
	RI2#	in	Serial port COM2 ring indicator
	RTS2#	out	Serial port COM2 request to send
	RXD2	in	Serial port COM2 receive data
	TXD2	out	Serial port COM2 transmit data
MPC8245 COM3/ COM4	RXD3	in	Serial port COM3 receive data (MPC8245)
	TXD3	out	Serial port COM3 transmit data (MPC8245)
	RXD4	in	Serial port COM4 receive data (MPC8245)
	TXD4	out	Serial port COM4 transmit data (MPC8245)
USB	USBP0+, USBP0-	in/out	USB port differential pair

1 Connect the anode to +5 V (pin 12 of 40-pin connector).
2 Connect the button's second terminal to GND (pin 11 of 40-pin connector).

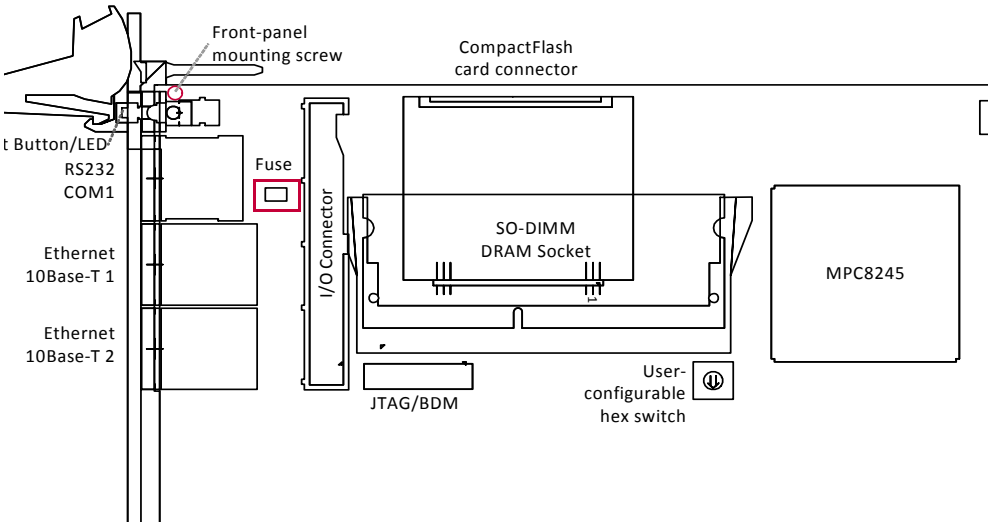
2.10.1 Fuse Protection

The I/O connector is protected by a fuse. **This fuse is not intended to be exchanged by the customer. Your warranty for the A15 will cease if you exchange the fuses on your own.** Please send your board to MEN for repair if a fuse blows.

- Current rating: 1.5 A
- Type: fast
- Size: 1206
- MEN part number: 5675-0001

The fuses are located on the top side of A15.

Figure 9. *Position of fuse for I/O connector protection*



2.11 Serial Ports COM1/COM2

The onboard Super I/O controller Ali M1543 provides two high-performance 16550 compatible UARTs with 16-byte send/receive FIFOs and a programmable baud rate generator. You can set the baud rate through MENMON.

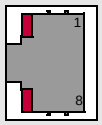
2.11.1 COM1/COM2 via Front Connector

COM1 and COM2 are standard RS232 interfaces led to an RJ45 connector at the front panel. On version A15B only COM1 is accessible at the front panel, while COM2 is available for SA-Adapter connection on the I/O connector (see Chapter 2.10 I/O Expansion Connector on page 42).

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

Table 9. *Pin assignment of 8-pin RJ45 RS232 connectors (COM1/COM2)*



1	DSR
2	DCD
3	DTR
4	GND
5	RXD
6	TXD
7	CTS
8	RTS

Note: The two LEDs integrated in the COM1 connector are user LEDs and have no function for the serial COM1 port! The COM2 connector does not have LEDs.

2.11.2 COM2 via onboard I/O Connector

On A15B the signal lines of COM2 are connected to the I/O connector (see Chapter 2.10 I/O Expansion Connector on page 42). You can use this interface with an SA-Adapter.

The signal level is fixed to TTL. This allows flexible line interface configuration using serial interface adapters (SA-Adapters). MEN offers a mounting kit for connection of standard SA-Adapters.

COM2 supports the use of any of MEN's standard SA-Adapters. This allows you to choose from a number of available line interfaces, from RS232 to RS422/RS485 to TTY, with or without optical isolation.

For compatible adapters and the mounting kit please see the A15B and A15C pages on MEN's website.

2.11.2.1 Installing Standard SA-Adapters

Note: MEN gives no warranty on functionality and reliability of the board and SA-Adapters used if you install SA-Adapters in a different way than described in this manual.

Perform the following steps to install standard SA-Adapters using MEN's mounting kit:

- ☑ Power-down your system and remove the board from the system.
- ☑ Remove the two front panel screws and the two screws on top of the mounting bolts of the SA-Adapter.

- ☑ Use the front panel screws to fasten the SA-Adapter at the additional SA-Adapter front panel.
- ☑ Plug the prefolded ribbon cable to the 40-pin I/O connector on the board.
- ☑ Plug the two 10-pin connector of the ribbon cable to the respective SA-Adapter connector.
- ☑ Make sure to always match the pins correctly (pin 1 is marked by a triangle on the ribbon cable connector).
- ☑ You can now reinsert the board and the additional front panel into your system. Make sure to fasten the SA-Adapter front panel appropriately in your enclosure!

2.12 Temperature Sensor

The LM75 temperature sensor is used for temperature management. It continuously measures the board temperature.

2.13 Real-Time Clock and NVRAM

The board includes the 41T56 SMB real-time clock with integrated NVRAM. A local GoldCap capacitor supplies the backup voltage. The real-time clock must be supplied via the VMEbus *STDBY* line.

The 56-byte NVRAM is organized as a 56 bytes x 8 bits SRAM.

2.14 Watchdog

The board uses an SMS24 watchdog, which has three functions:

- Power-On Reset
- Watchdog
- EEPROM (4 kbits) (see Chapter 2.5.4 EEPROM on page 30)

2.15 User LEDs

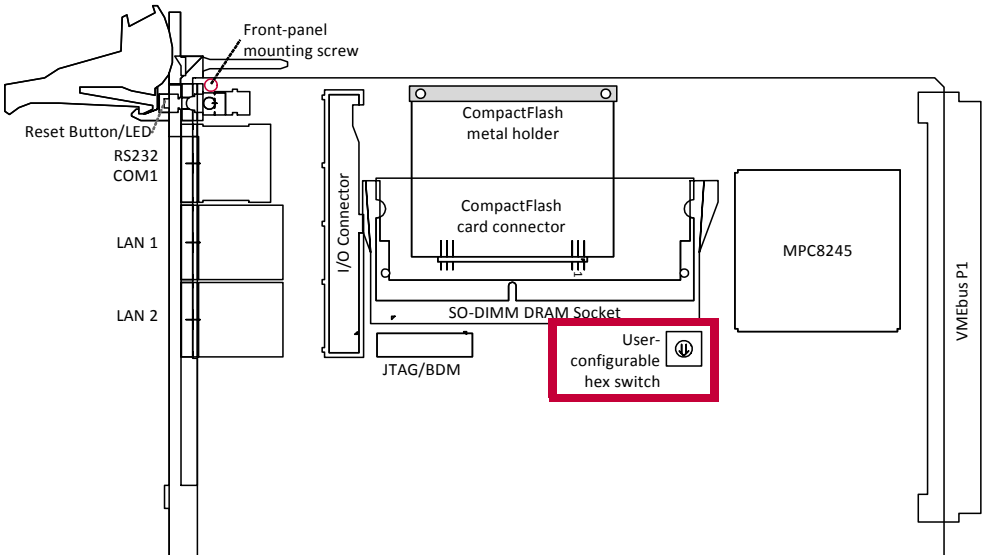
The A15 provides two user LEDs at the front-panel COM1 connector. The LEDs are led to the I/O connector. (Cf. Chapter 2.10 I/O Expansion Connector on page 42 and Chapter 2.11.1 COM1/COM2 via Front Connector on page 45.)

The LEDs are controlled through GPIO pins 4 and 5 of the ALI1543 controller.

2.16 User-Defined Hex Switch

The board provides a rotary hex switch for operating system requirements and user applications. Please refer to the corresponding software manual for their implementation.

Figure 10. *Position of Hex Switch*



2.17 VMEbus Interface

The A15's VMEbus interface conforms to the VMEbus specification. It has the following features:

- Slot-1 functionality with auto-detection
- Wide range of VMEbus address and data transfer modes
  - Master D08(EO):D16:D32:D64:A16:A24:A32:ADO:BLT:RMW
  - Slave D08(EO):D16:D32:D64:A16:A24:A32:BLT:RMW
- Interrupt handler: 7-level, D08(O):IH(7-1)
- Interrupter: 7-level, D08(O):I(7-1):ROAK
- Single level 3 fair requester
- Single level 3 arbiter
- BTO bus timeout
- DMA controller with scatter gather DMA (A32/D64)
- Mailbox functionality
- Location monitor A16, A24, A32
- Dual-ported system register
- Access to 1 MB shared fast SRAM or to PCI space

2.17.1 PCI Configuration Space Registers

The Configuration Registers from 0x00 to 0x3C conform with the PCI Device Configuration Header Format.

Table 10. *VMEbus interface PCI configuration space registers*

Address	Byte			
	3	2	1	0
0x00	Device ID (0x5056)		Vendor ID (0x1172)	
0x04	Status Register		Command Register	
0x08	Class Code (0x068000)			Revision ID (currently 0x01)
0x0C	BIST	Header Type	Latency Timer	Cache Line Size
0x10	Base Address Register 0			
0x14	Base Address Register 1			
0x18	Base Address Register 2			
0x1C	Base Address Register 3			
0x20	Base Address Register 4			
0x24	*This register is always 0.*			
0x28	Card Bus CIS Pointer			
0x2C	Subsystem ID (0x7A30)		Subsystem Vendor ID (0x3032)	
0x30	Expansion ROM Base Address Register			
0x34	Reserved			
0x38	Reserved			
0x3C	Maximum Latency	Minimum Grant	Interrupt Pin	Interrupt Line

2.17.2 Runtime Registers

The registers are accessible both from the PCI and the VMEbus side.

From the PCI-bus side the address is the value of BAR 0 (e.g. 0x 8800 0000) plus an offset (0x 0180 0000) plus the register address (e.g. 0x 0008 for ISTAT).

From the VMEbus side, the registers are accessible in A16 mode only. (E.g. slave base address A16 = 0x00001000, plus register address).

The Mailbox Data Registers and the DMA Buffer Descriptors are stored in the SRAM and can be accessed via the offset address of the SRAM. See Chapter 2.17.3 VMEbus Master Mapping on page 53, Chapter 2.17.4 VME Slave Mapping on page 54, Chapter 2.17.5 SRAM on page 54 and Table 12, Mailbox and DMA registers in SRAM, on page 52.

Note: If an application uses the whole SRAM space, the DMA and mailbox functions will not work!

Table 11. *VMEbus bridge control registers*

Address	D31..D0
0x 0000	INTR – VME Interrupt Control Register (r/w)
0x 0004	INTID – VME Interrupt STATUS/ID Register (r/w)
0x 0008	ISTAT – Interrupt Status Register (r)
0x 000C	IMASK – Interrupt Mask Register (r/w)
0x 0010	MSTR – Master Control Register (r/w)
0x 0014	SLV24 – Slave Control Register A24 (r/w)
0x 0018	SYSCTL – System Controller Register (r/w)
0x 001C	LONGADD – Upper 3 Address Bits for A32 (r/w)
0x 0020	MAIL_IRQE – Mailbox Interrupt Enable Register (r/w)
0x 0024	MAIL_IRQ – Mailbox Interrupt Request Register (r/w)
0x 002C	DMASTA – DMA Status Register (r/w)
0x 0030	SLV16 – Slave Control Register A16 (r/w)
0x 0034	SLV32 – Slave Control Register A32 (r/w)
0x 0038	LOCSTA_0 – Location Status Register (r/w)
0x 003C	LOCSTA_1 – Location Status Register (r/w)
0x 0040	LOCADDR_0 – Location Monitor Address Register (r/w)
0x 0044	LOCADDR_1 – Location Monitor Address Register (r/w)
0x 0048	SLV24_PCI – A24 Slave Base Address for PCI (r/w)
0x 004C	SLV32_PCI – A32 Slave Base Address for PCI (r/w)

Table 12. *Mailbox and DMA registers in SRAM*

Address	D31..D0
0x FF800	MAILBOX_0 – Mailbox Data Register (r/w)
0x FF804	MAILBOX_1 – Mailbox Data Register (r/w)
0x FF808	MAILBOX_2 – Mailbox Data Register (r/w)
0x FF80C	MAILBOX_3 – Mailbox Data Register (r/w)
0x FF900..FF90C	DMA_BD#1 – DMA Buffer Descriptor (r/w)
0x FF910..FF91C	DMA_BD#2 – DMA Buffer Descriptor (r/w)
.. 0x FFFF0..FFFFC	Further Buffer Descriptors

2.17.3 VMEbus Master Mapping

The PCI to VMEbus bridge uses BAR0 to access the VMEbus. BAR1 is used for VME A32/D32 accesses. BAR2 and BAR3 are equal to BAR0 and BAR1, but every VMEbus access is swapped. BAR4 contains swapped and non-swapped A24/D32 windows.

Table 13. *VMEbus interface BAR 0*

BAR0 **Internal:** 0x 0000 0000	**Size**	**Function**
0x 0000 0000 .. 0x 00FF FFFC	16 MB	VME A24 D16 (standard) space
0x 0100 0000 .. 0x 0100 FFFC	64 KB	VME A16 D16 (short) space
0x 0101 0000 .. 0x 0101 FFFC	64 KB	VME A16 D32 (short) space
0x 0140 0000 .. 0x 014F F7FF	1022 KB	Local SRAM
0x 014F F800 .. 0x 014F FFFC	2 KB	Mailbox Data Registers and DMA Buffer Descriptors (included in SRAM)
0x 0180 0000 .. 0x 0180 0044	72 bytes	VME Bridge Control Registers
0x 01C0 0000	16 bytes	VME IACK space

Table 14. *VMEbus interface BAR1*

BAR1 **Internal:** 0x 8000 0000	**Size**	**Function**
0x 0000 0000 .. 0x 1FFF FFFC	512 MB	VME A32 D32 (long) space

Table 15. *VMEbus interface BAR2*

BAR2 **Internal:** 0x 0000 0001	**Size**	**Function**
0x 0000 0000 .. 0x 00FF FFFC	16 MB	VME A24 D16 (standard) space **swapped**
0x 0100 0000 .. 0x 0100 FFFC	64 KB	VME A16 D16 (short) space **swapped**
0x 0101 0000 .. 0x 0101 FFFC	64 KB	VME A16 D32 (short) space **swapped**
0x 0140 0000 .. 0x 014F F7FF	1022 KB	Local SRAM
0x 014F F800 .. 0x 014F FFFC	2 KB	Mailbox Data Registers and DMA Buffer Descriptors (included in SRAM)
0x 0180 0000 .. 0x 0180 0044	72 bytes	VME Bridge Control Registers

Table 16. *VMEbus interface BAR3*

BAR3 **Internal:** 0x 8000 0001	**Size**	**Function**
0x 0000 0000 .. 0x 1FFF FFFC	512 MB	VME A32 D32 (long) space **swapped**

Table 17. VMEbus interface BAR4

BAR4 Internal: 0x C000 0000 and 0x C000 0001	Size	Function
0x 0000 0000 .. 0x 00FF FFFC	16 MB	VME A24 D32 (standard) space
0x 0100 0000 .. 0x 01FF FFFC	16 MB	VME A24 D32 (standard) space **swapped**

2.17.4 VME Slave Mapping

The PCI space, 1 MB SRAM, the internal RAM and all registers are accessible by the VMEbus. The registers and the internal RAM is a 4-kB block, which is accessible in A16 mode only. This block is mapped to the slave base address for A16 mode. The SRAM can be mapped to the A24 and A32 base address, whereas the SRAM is mirrored in A32 mode. The PCI space is also mapped to the A24 and A32 space. The size of the A24/A32 windows is configurable in the corresponding Mask Registers.

Table 18. VMEbus slave address windows

VME Slave Access	Size	Address	Function
A16	72 bytes	0x 000 .. 0x 044	VME Bridge Control Registers
A24	1022 KB	0x 0 0000 .. 0x F F7FF	Local SRAM
	2 KB	0x F F800 .. 0x F FFFC	Mailbox Data Registers and DMA Buffer Descriptors (included in SRAM)
	64 KB.. 1 MB	0x 0 0000 .. 0x F FFFC	PCI Space
A32	1022 KB	0x 0 0000 .. 0x F F7FF	Local SRAM
	2 KB	0x F F800 .. 0x F FFFC	Mailbox Data Registers and DMA Buffer Descriptors
	1 MB.. 256 MB	0x 0000 0000 .. 0x 000F FFFC	PCI Space

Note: The registers for mailbox and DMA are located in the SRAM (0xFF 800 to 0xFF FFFF). If an application uses the whole SRAM space, the DMA and mailbox functions will not work!

2.17.5 SRAM

The SRAM is accessible from the PCI and VMEbus side. From the VMEbus side, the base address is defined in the Slave Control Registers for A24 or A32 (in A32 mode the SRAM is mirrored!).

The SRAM has a size of 1 MB. It is accessible via block and standard transfers (user and supervisor space).

2.17.6 Slot-1 Function

The slot-1 function is auto-detected. It can be read from the SYSCTL register (bit *SYSCON*). The A15 samples *BG3IN#* after *SYSRES#* has gone high. As specified in the VMEbus specification all *BG* lines should be high after reset. Therefore only in slot 1 */BG3IN* can be sampled low, due to a local pull-down resistor.

After slot 1 is detected the functions listed below are enabled.

- Generation of *SYSRES#*
- Generation of *SYSCLK* (not provided during slot 1 detection cycle)
- Level 3 arbitration
- Bus arbitration timeout 250 µs
- Bus transfer timeout 125 µs

The timeouts cannot be changed.

SYSCTL – System Controller Register (0x0018) (read/write)

7..3	2	1	0
-	ATO	SYSRES	SYSCON

ATO Monitor for arbitration timeout signal (read only)

0 = No arbitration timeout (default)
1 = Arbitration timeout occurred (cleared by writing 1)

SYSRES Reset VMEbus; generates *SYSRES#* on the VMEbus

0 = *SYSRES#* active (can be activated when *SYSCON*=1)
1 = *SYSRES#* not active

SYSCON System controller status (depends on slot 1 auto-detection after reset). May be overridden by software. Independent of the *SYSCON* bit, a *SYSRES* on the VMEbus will result in a reset, which will be routed to the local CPU.

0 = Slot 1 function disabled
1 = Slot 1 function enabled

2.17.7 VMEbus Master Interface

The A15 VMEbus master interface converts PCI bus cycles to VMEbus cycles.

The read/write cycles are performed in the A16, A24 and A32 address ranges of the VMEbus. D08(E/O), D16 and D32 transfers will be executed. D64 transfers are only possible with the DMA controller. The MSTR – Master Control Register (0x0010) (read/write) enables the A15 to generate single RMW transfers or Address-Only cycles.

MSTR – Master Control Register (0x0010) (read/write)

7..6	5	4	3	2	1	0
-	AONLY	POSTWR	IBERREN	BERR	REQ	RMW

AONLY Enable single address only cycle

0 = Normal cycle (default)
1 = Adress only cycle

The master does not transfer data with this cycle. Other slaves can detect this cycle to generate local interrupts.
Only 8-bit or 16-bit read cycles are allowed for address-only cycles!
This bit will be reset after the transmission was done.

POSTWR Posted Write Access to VMEbus (not supported)

0 = Delayed write access to VMEbus (default)
1 = Posted write access to VMEbus

IBERREN Interrupt Bus Error Enable

0 = Local interrupt disabled if VMEbus bus error occurs (default)
1 = Local interrupt enabled if VMEbus bus error occurs

BERR Monitor for VMEbus *BERR#* signal

0 = No VMEbus error (default)
1 = VMEbus error occurred; *BERR#* signal asserted. Cleared by writing 1.

REQ Set VMEbus requester scheme

0 = Request scheme for VMEbus master and interrupt handler is set to Release On Request (ROR) (default)
1 = Request scheme is set to Release When Done (RWD)

If this bit is changed from 0 to 1, i. e. from ROR to RWD, and there were previous accesses over the master interface, it is recommended to do a dummy read to free the bus.

RMW Enable single Read-Modifiy-Write cycle

0 = Normal cycle (default)
1 = RMW cycle. Master keeps *AS#* asserted during back-to-back read/ write cycle.

This bit is automatically cleared after the RMW cycle and must be set for the next RMW cycle again.

The following master/slave RMW accesses are allowed:

- Byte or word access in D16 mode
- Byte, word or long access in D32 mode

Note: During RMW cycles all interrupts on the host CPU should be masked.

In order to do a RMW cycle, the right order must be considered: First set the RMW bit in the MSTR register. Now, a read transaction on VMEbus can be done (no long access on D16 spaces!). When the read was done, the bus is blocked until the write access will be performed. In order not to interfere with the RMW order, all other VME master actions should be blocked by software (DMA should not be active!).

Transfers in D32 mode are done within one VME cycle. If a long access is performed to a D16 address space, the VMEbus master will do two word accesses in order to transmit 32 bits. These two accesses are not dividable by other VME masters!

The following table lists all valid combinations for byte enables supported by the bridge. Note that even within a PCI burst transfer the byte enables may change from one data portion to the next. This must be taken into account when exchanging data with the SRAM.

Table 19. *VMEbus interface valid combinations for byte enables supported by PCI-to-VME bridge*

PCI Bus (always dword aligned address[1])				Byte Lane Mapping 32-bit PCI 64-bit VME	VMEbus (always word aligned address)			
Byte Enables								
3	2	1	0		DS1	DS0	A1	LW
D16								
1	1	1	1	No transfers	x	x	x	x
1	1	1	0	D7..D0 ⇔ D15..D8	0	1	0	1
1	1	0	1	D15..D8 ⇔ D7..D0	1	0	0	1
1	0	1	1	D23..D16 ⇔ D15..D8	0	1	1	1
0	1	1	1	D31..D24 ⇔ D7..D0	1	0	1	1
1	1	0	0	D7..D0 ⇔ D15..D8 D15..D8 ⇔ D7..D0	0	0	0	1
0	0	1	1	D23..D16 ⇔ D15..D8 D31..D24 ⇔ D7..D0	0	0	1	1
1	0	1	0	First: D23..D16 ⇔ D15..D8 Second: D7..D0 ⇔ D15..D8	0 0	1 1	1 0	1
0	1	0	1	First: D31..D24 ⇔ D7..D0 Second: D15..D8 ⇔ D7..D0	1 1	0 0	1 0	1
0	1	1	0	First: D31..D24 ⇔ D7..D0 Second: D7..D0 ⇔ D15..D8	1 0	0 1	1 0	1
1	0	0	1	First: D23..D16 ⇔ D15..D8 Second: D15..D8 ⇔ D7..D0	0 1	1 0	1 0	1
1	0	0	0	First: D23..D16 ⇔ D15..D8 Second: D7..D0 ⇔ D15..D8 D15..D8 ⇔ D7..D0	0 0	1 0	1 0	1
0	0	0	1	First: D23..D16 ⇔ D15..D8 D31..D24 ⇔ D7..D0 Second: D15..D8 ⇔ D7..D0	0 1	0 0	1 0	1
0	1	0	0	First: D31..D24 ⇔ D7..D0 Second: D7..D0 ⇔ D15..D8 D15..D8 ⇔ D7..D0	1 0	0 0	1 0	1
0	0	1	0	First: D31..D24 ⇔ D7..D0 D23..D16 ⇔ D15..D8 Second: D7..D0 ⇔ D15..D8	0 0	0 1	1 0	1
0	0	0	0	First: D23..D16 ⇔ D15..D8 D31..D24 ⇔ D7..D0 Second: D7..D0 ⇔ D15..D8 D15..D8 ⇔ D7..D0	0	0	1 0	1

PCI Bus (always dword aligned address[1])				Byte Lane Mapping 32-bit PCI 64-bit VME	VMEbus (always word aligned address)			
Byte Enables								
3	2	1	0		DS1	DS0	A1	LW
D32								
1	0	0	1	D15..D8 ⇔ D23..D16 D23..D16 ⇔ D15..D8	0	0	1	0
0	0	0	1	D15..D8 ⇔ D23..D16 D23..D16 ⇔ D15..D8 D31..D24 ⇔ D7..D0	1	0	0	0
1	0	0	0	D7..D0 ⇔ D31..D24 D15..D8 ⇔ D23..D16 D23..D16 ⇔ D15..D8	0	1	0	0
0	0	0	0	D7..D0 ⇔ D31..D24 D15..D8 ⇔ D23..D16 D23..D16 ⇔ D15..D8 D31..D24 ⇔ D7..D0	0	0	0	0
D64								
0	0	0	0	D7..D0 ⇔ D63..D56 D15..D8 ⇔ D55..D48 D23..D16 ⇔ D47..D40 D31..D24 ⇔ D39..D32 D39..D32 ⇔ D31..D24 D47..D40 ⇔ D23..D16 D55..D48 ⇔ D15..D8 D63..D56 ⇔ D7..D0	0	0	0	0

[1] PCI address bits A1 and A0 are only examined during I/O reads and writes. During memory reads and writes (as is the case here) these are always 0.

2.17.7.1 Address Modifiers

Table 20. *VMEbus master Address Modifier codes*

Hex Code	AM						Function
	5	4	3	2	1	0	
0x08	L	L	H	L	L	L	A32 non-privileged 64-bit block transfer (MBLT)
0x09	L	L	H	L	L	H	A32 non-privileged data access
0x0B	L	L	H	L	H	H	A32 non-privileged 32-bit block transfer (BLT)
0x29	H	L	H	L	L	H	A16 non-privileged access
0x39	H	H	H	L	L	H	A24 non-privileged data access
0x3B	H	H	H	L	H	H	A24 non-privileged 32-bit block transfer (BLT)

2.17.7.2 Bus Errors

If a bus error occurs, bit *BERR* in the MSTR – Master Control Register (0x0010) (read/write) is set. An interrupt is triggered if the *IBERREN* Bit in the MSTR – Master Control Register (0x0010) (read/write) is set. The timeout for *BERR* is 60 µs. The bus error can be cleared by writing 1 to the *BERR* bit.

2.17.7.3 Atomic Operations

CPU-to-SRAM Operations

Not supported.

CPU-to-VME Operations

Read-Modify-Write operations to the VMEbus can be done via bit *RMW* in the MSTR – Master Control Register (0x0010) (read/write). Only byte and word accesses are allowed, with word accesses being made to even addresses.

VME-to-SRAM Operations

Supported.

2.17.8 VMEbus Slave Interface

The slave interface consists of 1 MB dual-ported high-speed SRAM. Block transfer (BLT) is performed with a transfer rate of up to 25 MB/s (theoretically). RMW cycles are supported by the slave interface to the SRAM. During an RMW cycle to the SRAM, a PCI access to the SRAM is blocked.

The A16, A24 and A32 base addresses are defined in the Slave Control Registers. On simultaneous access by a VMEbus master and the local CPU the VMEbus master has the highest priority.

The Slave Base Address must be aligned to the chosen size of the window.

SLV24 – Slave Control Register A24 (0x0014) (read/write)

15..12	11..8
SLMASK24[19:16]	SLBASE24[19:16]

7..5	4	3..0
	SLEN24	SLBASE24[23:20]

SLMASK24 Slave Base Address Mask Bits. The size of the A24 Slave window can be set to:

0000 = 1 MB
1000 = 512 KB
1100 = 256 KB
1110 = 128 KB
1111 = 64 KB

Default: 0000

SLEN24 0 = Slave Unit disabled (default)
1 = Slave Unit enabled

SLBASE24 Slave's Base Address. Specifies the lowest address in the VME address range that will be decoded. Since only A[23:20] are monitored, the smallest possible address space is 64 KB.
Default: 0000

SLV16 – Slave Control Register A16 (0x0030) (read/write)

7..5	4	3..0
	SLEN16	SLBASE16

SLEN16 0 = Slave Unit disabled (default)
1 = Slave Unit enabled

SLBASE16 Slave's Base Address. Specifies the lowest address in the VME address range that will be decoded. Since only A[15:12] are monitored, the smallest possible address space is 4 KB.
Default: 0000

SLV32 – Slave Control Register A32 (0x0034) (read/write)

23..16
SLMASK32[27:20]

15..8
SLBASE32[27:20]

7..5	4	3..0
	SLEN32	SLBASE32[31:28]

SLMASK32 Slave Base Address Mask Bits. The size of the A32 Slave window can be set to:

00000000 = 256 MB
10000000 = 128 MB
11000000 = 64 MB
11100000 = 32 MB
11110000 = 16 MB
11111000 = 8 MB
11111100 = 4 MB
11111110 = 2 MB
11111111 = 1 MB

Default: 00000000

SLEN32 0 = Slave Unit disabled (default)
1 = Slave Unit enabled

SLBASE32 Slave's Base Address. Specifies the lowest address in the VME address range that will be decoded. Since only A[31:28] are monitored, the smallest possible address space is 1 MB.
Default: 000000000000

SLV24_PCI – Slave Control Register A24 for PCI Access (0x0048) (read/write)

15..12	11..8
SLMASK24_PCI[19:16]	SLBASE24_PCI[19:16]

7..5	4	3..0
	SLEN24_PCI	SLBASE24_PCI[23:20]

SLMASK24_PCI Slave Base Address Mask Bits. The size of the A24 PCI Slave window can be set to:

0000 = 1 MB
1000 = 512 KB
1100 = 256 KB
1110 = 128 KB
1111 = 64 KB

Default: 0000

SLEN24_PCI 0 = Slave Unit disabled (default)
1 = Slave Unit enabled

SLBASE24_PCI Slave's Base Address for PCI access. Specifies the lowest address in the VME address range that will be decoded. Since only A[23:16] are monitored, the smallest possible address space is 64 KB.
Default: 00000000

SLV32_PCI – Slave Control Register A32 for PCI Access (0x004C) (read/write)

23..16
SLMASK32_PCI[27:20]

15..8
SLBASE32_PCI[27:20]

7..5	4	3..0
	SLEN32_PCI	SLBASE32_PCI[31:28]

SLMASK32_PCI Slave Base Address Mask Bits. The size of the A32 PCI Slave window can be set to:

00000000 = 256 MB
10000000 = 128 MB
11000000 = 64 MB
11100000 = 32 MB
11110000 = 16 MB
11111000 = 8 MB
11111100 = 4 MB
11111110 = 2 MB
11111111 = 1 MB

Default: 00000000

SLEN32_PCI 0 = Slave Unit disabled (default)
1 = Slave Unit enabled

SLBASE32_PCI Slave's Base Address for PCI access. Specifies the lowest address in the VME address range that will be decoded. Since only A[31:20] are monitored, the smallest possible address space is 1 MB.
Default: 000000000000

PCI_Offset – PCI Offset Address (0x0028) (read/write)

31..12	11..0
PCI_OFFSET[31:12]	0

PCI_OFFSET 4-kbyte aligned offset address on PCI bus for VME-to-PCI accesses.

The PCI space is accessible via A24 and A32 access on the VMEbus. To do this, the SLV24_PCI or SLV32_PCI control registers must be set.

2.17.8.1 Address Modifiers

Table 21. *VMEbus slave Address Modifier codes*

Hex Code	AM						Function
	5	4	3	2	1	0	
0x3F	H	H	H	H	H	H	A24 Standard supervisory block transfer
0x3D	H	H	H	H	L	H	A24 Standard supervisory data access
0x3B	H	H	H	L	H	H	A24 Standard non-privileged block transfer
0x39	H	H	H	L	L	H	A24 Standard non-privileged data access
0x3C	H	H	H	H	L	L	A24 supervisory 64-bit block transfer (MBLT)
0x38	H	H	H	L	L	L	A24 non-privileged 64-bit block transfer (MBLT)
0x29	H	L	H	L	L	H	A16 non-privileged access
0x2D	H	L	H	H	L	H	A16 supervisory data access
0x0F	L	L	H	H	H	H	A32 supervisory block transfer (BLT)
0x0D	L	L	H	H	L	H	A32 supervisory data access
0x0C	L	L	H	H	L	L	A32 supervisory 64-bit block transfer (MBLT)
0x0B	L	L	H	L	H	H	A32 non-privileged block transfer (BLT)
0x09	L	L	H	L	L	H	A32 non-privileged data access
0x08	L	L	H	L	L	L	A32 non-privileged 64-bit block transfer (MBLT)

2.17.9 VMEbus Requester

Bus requests are executed at bus request level 3. No other levels are available. The requester uses the Release-On-Request (ROR) or Release-When-Done (RWD) scheme. ROR should be preferred in single VMEbus master systems to increase the transfer rate. Both register schemes are implemented as fair requester.

Settings are made in the MSTR – Master Control Register (0x0010) (read/write). See Chapter 2.17.7 VMEbus Master Interface on page 56.

Unused daisy-chain lines are passed by (*BG0IN#/OUT#, BG1IN#/OUT#, BG2IN#/OUT#*).

2.17.10 VMEbus Interrupt Handler

The board can receive interrupts on all seven levels. In addition, it can handle *ACFAIL#* interrupts. You can mask interrupts through the IMASK – Interrupt Mask Register (0x000C) (read/write). The interrupts are not prioritized.

If a VME interrupt occurs that is not masked, the PCI-to-VME bridge generates a PCI interrupt (routed to INT_B on board). Then, the software must read the ISTAT – Interrupt Status Register (0x0008) (read/write) to detect which VME interrupts are pending. The ISTAT register will only show bits that were enabled in IMASK!

The interrupt vector must then be fetched through a read to the VME IACK space. The address within the IACK space must reflect the VMEbus level (e.g. word access 0xA or byte access 0xB for level 5).

Naturally, there is no vector for ACFAIL interrupts. To reset such interrupts, write 1 to the *ACFST* bit in ISTAT – Interrupt Status Register (0x0008) (read/write).

IMASK – Interrupt Mask Register (0x000C) (read/write)

7	6	5	4	3	2	1	0
IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	ACFEN

IENx If the corresponding interrupt pin *IRQx* is asserted, the bridge will signal an interrupt to the PCI side (*INTB#*).

0 = Interrupt masked (default)
1 = Interrupt enabled

ACFEN When this bit is set, and *ACFAIL#* is detected, an interrupt on the PCI side is generated.

0 = Interrupt masked (default)
1 = *ACFAIL#* interrupt enabled

ISTAT – Interrupt Status Register (0x0008) (read/write)

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	ACFST

Ix The PCI Master can read the asserted interrupts here. These are not stored here, they can just be read here. Interrupts are reset automatically if the external interrupter removes its request. Writes to these bits are ignored.

ACFST If this reads 1, an *ACFAIL#* interrupt has occurred. This interrupt is stored, because it is not static. It can be cleared by writing 1.
Default: 0

In order to read the interrupt STATUS/ID from the interrupter, the CPU must generate a read cycle to the IACK memory area by setting the last significant address bits A[3..1] to the corresponding interrupt level (e. g. for IRQ5# set A[3:1] to [101]).

2.17.11 VMEbus Interrupter

The board has one interrupter. It can generate an interrupt on all seven levels, but only one at a time. The interrupt level is selected in the INTR – VME Interrupter Control Register (0x0000) (read/write). The associated interrupt status ID, which is provided to the interrupt handler during the IACK cycle, is stored in the INTID – VME Interrupt STATUS/ID Register (0x0004) (read/write). The interrupt request is auto cleared after an IACK cycle (ROAK).

INTR – VME Interrupter Control Register (0x0000) (read/write)

7..4	3	2	1	0
-	INTEN	IL2	IL1	IL0

This register controls the internal interrupter. Interrupt levels from 1 to 7 can be set. The interrupt is generated only when the *INTEN* bit is set.

INTEN Interrupter enable

0 = Interrupt disabled (default)
1 = Enable interrupt at level specified through *ILx*

The interrupt level is set in binary code (e. g. *ILx*=011 is IRQ3).
Default: 0x0

ILx Interrupter request level

The level is set by a binary value of a 3-to-7 demultiplexer (e.g. IL[2:0]=011 is IRQ3).

Default: 0x0

INTEN should be set after the *ILx* bits are set to avoid glitches on the IRQ lines.

INTEN is automatically cleared during the acknowledge cycle and the request is removed (ROAK). The *ILx* bits, however, remain set until they are overwritten.

Check the *INTEN* bit to verify that the interrupt has been acknowledged.

INTID – VME Interrupt STATUS/ID Register (0x0004) (read/write)

7..0
INT_ID

In this register, the STATUS/ID of the internal interrupter is set.

INT_ID The STATUS/ID of the interrupt that the external handler reads during the IACK cycle.
Default: 0x00

2.17.12 A32 Address Mode

Since the address space for BAR1 is limited to 512 MB, the upper three address bits must be set in another way, in order to address the entire VMEbus address space. Therefore, a register contains the upper three address bits.

LONGADD – Upper 3 Address Bits for A32 (0x001C) (read/write)

7..3	2	1	0
-	ADDR31	ADDR30	ADDR29

ADDR31..ADDR29 Upper 3 address bits for A32 access. These bits will be combined with the address bits ADDR28..ADDR2 while an A32 access on the VMEbus is performed, in order to address the entire A32 space.

2.17.13 Mailbox

You can use the mailbox feature to send messages without using the slow interrupt daisy chain. Writing and/or reading one of the data registers of the mailbox from the VMEbus side generates a local interrupt.

MAIL_IRQE – Mailbox Interrupt Enable Register (0x0020) (read/write)

7	6	5	4	3	2	1	0
IEVW3	IEVR3	IEVW2	IEVR2	IEVW1	IEVR1	IEVW0	IEVR0

IEVWx VMEbus write access to mailbox register *x* generates an interrupter request on the PCI-bus when this bit is set.

Default: 0x0 (interrupt disabled)

This bit can be set and reset from both sides (PCI side and VMEbus side). If both sides access this bit, the VMEbus side wins.

IEVRx VMEbus read access to mailbox register *x* generates an interrupter request on the PCI-bus side when this bit is set.

Default: 0x0 (interrupt disabled)

This bit can be set and reset from both sides (PCI side and VMEbus side). If both sides access this bit, the VMEbus side wins.

MAIL_IRQ – Mailbox Interrupt Request Register (0x0024) (read/write)

7	6	5	4	3	2	1	0
IPVW3	IPVR3	IPVW2	IPVR2	IPVW1	IPVR1	IPVW0	IPVR0

IPVWx Interrupter pending on the PCI bus because of VMEbus write access to mailbox register *x*. Cleared by writing 1.

Note: Any IRQ bit will only be set if the corresponding enable bit is set!

IPVRx Interrupter pending on the PCI bus because of VMEbus read access to mailbox register *x*. Cleared by writing 1.

Default: 0x0 (no interrupt pending)

This bit can be cleared from both sides.

MAILBOX_0..MAILBOX_3 – Mailbox Data Register (0xFF800, 0xFF804, 0xFF808, 0xFF80C) (read/write)

31..0
Data

Writing or reading this register results in an interrupt in the MAIL_IRQ – Mailbox Interrupt Request Register (0x0024) (read/write), if the interrupt is enabled in the MAIL_IRQE – Mailbox Interrupt Enable Register (0x0020) (read/write).

This data register can be used to transmit a status or ID.

2.17.14 Location Monitor

The location monitor is used to monitor the VMEbus. If the ongoing address and VMEbus access is identical to the configured one, an interrupt will be generated.

LOCSTA_0 – Location Status Register (0x0038) (read/write)

7	6	5	4	3	2..1	0
ADDR_4	ADDR_3	LOC_ WR_0	LOC_ RD_0	LOC_ STAT_0	LOC_AM_0	LOC_ IRQE_0

LOCSTA_1 – Location Status Register (0x003C) (read/write)

7	6	5	4	3	2	0
ADDR_4	ADDR_3	LOC_ WR_1	LOC_ RD_1	LOC_ STAT_1	LOC_AM_1	LOC_ IRQE_1

ADDR_4..3 Address bits 4 and 3 of VMEbus address; stored when location monitor found hit

LOC_WR_x
0 = Write accesses are not monitored
1 = Write accesses are monitored

LOC_RD_x
0 = Read accesses are not monitored
1 = Read accesses are monitored

LOC_STAT_x Location monitor status (interrupt request if enabled): If set, the address and address mode on the VMEbus are identical to *LOCADDR_x* and *LOC_AM_x*.

Reset by writing 1.

LOC_AM_x Monitor Address Mode

0 0 = A32 - Address bits [31:10] on VMEbus will be compared with *LOCADDR_x* [31:10]
0 1 = No function
1 0 = A16 - Address bits [15:10] on VMEbus will be compared with *LOCADDR_x* [15:10]
1 1 = A24 - Address bits [23:10] on VMEbus will be compared with *LOCADDR_x* [23:10]

LOC_IRQE_x
0 = Monitor interrupt request is disabled
1 = Monitor interrupt request is enabled

LOCADDR_0 – Location Monitor Address Register (0x0040) (read/write)

31..0
ADDR[31:0]

ADDR[31:0] Compare address for location monitor

The desired address bits depend on *LOC_AM_0*:

LOC_AM_0 = 0 0: *LOCADDR_0* [31:10]
LOC_AM_0 = 1 0: *LOCADDR_0* [15:10]
LOC_AM_0 = 1 1: *LOCADDR_0* [23:10]

LOCADDR_1 – Location Monitor Address Register (0x0044) (read/write)

31..0
ADDR[31:0]

ADDR[31:0] Compare address for location monitor

The desired address bits depend on *LOC_AM_1*:

LOC_AM_1 = 0 0: *LOCADDR_1* [31:10]
LOC_AM_1 = 1 0: *LOCADDR_1* [15:10]
LOC_AM_1 = 1 1: *LOCADDR_1* [23:10]

2.17.15 DMA Controller

The PLD has a DMA controller for high performance data transfer between the SDRAM and VMEbus. It is operated through a series of registers that control the source and destination for the data, length of the transfer and the transfer protocol to be used. These registers are not directly accessible, but they will be loaded with the contents of the internal memory.

A block of DMA registers stored in internal memory is called a buffer descriptor. A buffer descriptor may be linked to the next buffer descriptor, such that when the DMA has completed the operations described by one buffer descriptor, it automatically moves on to the next buffer descriptor in the external RAM list. The last buffer descriptor is reached, when the *DMA_NULL* bit is set in the corresponding buffer descriptor. The maximum number of buffer descriptors is 16.

The DMA controller is able to transfer data from the SDRAM to the VMEbus and vice versa. For this reason source and/or destination address can be incremented or not – depending on the settings. The source and destination address must be 8-byte aligned to each other.

The scatter-gather lists must be located in the local SRAM area. So a DMA can also be initiated by an external VME master.

DMASTA – DMA Status Register (0x002C) (read/write)

7..4	3	2	1	0
DMA_ACT_BD	DMA_ERR	DMA_IRQ	DMA_IEN	DMA_EN

This register contains the DMA interrupt and status bits.

DMA_ACT_BD Shows the number of the active buffer descriptor (read only)
If this bit is 0 and *DMA_EN* is 0, then the DMA controller is not working

DMA_ERR Will be asserted if a VMEbus error has occurred or if the DMA transaction has been stopped manually.
0 = DMA no error occurred
1 = DMA error occurred (reset by writing 1)

DMA_IRQ 0 = DMA IRQ inactive
1 = DMA IRQ active: transaction is done (reset by writing 1)

DMA_IEN 0 = DMA IRQ is disabled
1 = DMA IRQ is enabled

DMA_EN 0 = DMA transaction is stopped (or will be stopped if set to 0)
1 = DMA transaction is enabled (will be set to 0 when done)

DMA_BD#*x* – DMA Buffer Descriptors (0x0XX0..0XXC)

0x00	31..2	1..0
	DMA_DEST_ADDR	-

0x04	31..2	1..0
	DMA_SOUR_ADDR	-

0x08	31..16	15..0
	-	DMA_SIZE

	31..19	18..16	15	14..12	11..8	7..4	3	2	1	0
0x0C	-	DMA_ SOUR_ DEVICE	-	DMA_ DEST_ DEVICE	-	DMA_ VME_AM	-	INC_ SOUR	INC_ DEST	DMA_ NULL

DMA_DEST_ADDR Destination address of DMA transfer

DMA_SOUR_ADDR Source address of DMA transfer

DMA_SIZE Block size of DMA transfer in 4*bytes (max. 256 kB)

DMA_SOUR_DEVICE
0 0 1 = Source is located in SRAM address space
0 1 0 = Source is located in VME address space
1 0 0 = Source is located in PCI address space (not supported)

DMA_DEST_DEVICE
0 0 1 = Destination is located in SRAM address space
0 1 0 = Destination is located in VME address space
1 0 0 = Destination is located in PCI address space (not supported)

DMA_VME_AM VME address modifier for DMA transaction

0 0 0 0 = A24 D16 (DMA_x_ADDR [23:3] is used)
0 1 0 0 = A24 D32 (DMA_x_ADDR [23:3] is used)
0 1 1 0 = A32 D32 (DMA_x_ADDR [31:3] is used)
1 1 1 0 = A32 D64 (DMA_x_ADDR [31:3] is used)
0 0 0 1 = A24 D16 swapped
0 1 0 1 = A24 D32 swapped
0 1 1 1 = A32 D32 swapped
1 1 1 1 = A32 D64 swapped

INC_SOUR
0 = Increment source address during operation
1 = Keep source address

INC_DEST
0 = Increment destination address during operation
1 = Keep destination address

DMA_NULL
0 = End is not yet reached
1 = End of buffer descriptor list is reached

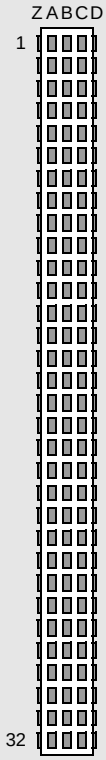
2.17.16 Connection

Connector types:

- 160-pin, 5-row plug, performance level according to DIN41612, part 5
- Mating connector:
  160-pin, 5-row receptacle, performance level according to DIN41612, part 5

The pin assignment of P1 conforms to the VME64 specification VITA 1-1994 and VME64 Extensions Draft Standard VITA 1.1-199x.

Table 22. *Pin assignment of VME64 connector P1*

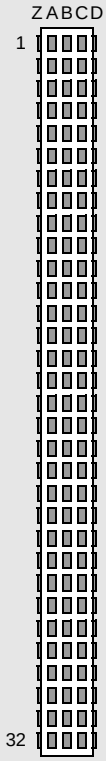


	Z	A	B	C	D
1	-	D0	BBSY#	D8	-
2	GND	D1	BCLR#	D9	GND
3	-	D2	ACFAIL#	D10	-
4	GND	D3	BG0IN#	D11	-
5	-	D4	BG0OUT#	D12	-
6	GND	D5	BG1IN#	D13	-
7	-	D6	BG1OUT#	D14	-
8	GND	D7	BG2IN#	D15	-
9	-	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	-	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	-
13	-	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	-
15	-	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	-
17	-	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	-
19	-	GND	AM3	A19	-
20	GND	IACK#	GND	A18	-
21	-	IACKIN#	-	A17	-
22	GND	IACKOUT#	-	A16	-
23	-	AM4	GND	A15	-
24	GND	A7	IRQ7#	A14	-
25	-	A6	IRQ6#	A13	-
26	GND	A5	IRQ5#	A12	-
27	-	A4	IRQ4#	A11	-
28	GND	A3	IRQ3#	A10	-
29	-	A2	IRQ2#	A9	-
30	GND	A1	IRQ1#	A8	-
31	-	-12V	VSTBY	+12V	-
32	GND	+5V	+5V	+5V	-

2.17.16.1 Pin Assignment of P2

The pin assignment of P2 depends on the board version of A15. In every version, P2 provides rear I/O for the mezzanine modules. A15B (M-Modules) also provides IDE and other signals.

Table 23. *Pin assignment of VMEbus rear I/O connector P2 – A15B – M-Modules*



	Z	A	B	C	D
1	FPGA8	Mod2 P2-2	+5V	Mod2 P2-1	IDE_RD[0]
2	GND	Mod2 P2-4	GND	Mod2 P2-3	IDE_RD[1]
3	FPGA7	Mod2 P2-6	-	Mod2 P2-5	IDE_RD[2]
4	GND	Mod2 P2-8	A24	Mod2 P2-7	IDE_RD[3]
5	Mod2 P2-22	Mod2 P2-10	A25	Mod2 P2-9	IDE_RD[4]
6	GND	Mod2 P2-12	A26	Mod2 P2-11	IDE_RD[5]
7	Mod2 P2-23	Mod2 P2-14	A27	Mod2 P2-13	IDE_RD[6]
8	GND	Mod2 P2-16	A28	Mod2 P2-15	IDE_RD[7]
9	Mod2 P2-24	Mod2 P2-18	A29	Mod2 P2-17	IDE_RD[15]
10	GND	Mod2 P2-20	A30	Mod2 P2-19	IDE_RD[14]
11	FPGA6	Mod1 P2-1	A31	Mod2 P2-21	IDE_RD[13]
12	GND	Mod1 P2-3	GND	Mod1 P2-2	IDE_RD[12]
13	FPGA5	Mod1 P2-5	+5V	Mod1 P2-4	IDE_RD[11]
14	GND	Mod1 P2-7	D16	Mod1 P2-6	IDE_RD[10]
15	FPGA4	Mod1 P2-9	D17	Mod1 P2-8	IDE_RD[9]
16	GND	Mod1 P2-11	D18	Mod1 P2-10	IDE_RD[8]
17	Mod1 P2-22	Mod1 P2-13	D19	Mod1 P2-12	IDE_RACT#
18	GND	Mod1 P2-15	D20	Mod1 P2-14	IDE_RCS1#
19	Mod1 P2-23	Mod1 P2-17	D21	Mod1 P2-16	IDE_RA[0]
20	GND	Mod1 P2-19	D22	Mod1 P2-18	IDE_RA[1]
21	Mod1 P2-24	Mod1 P2-21	D23	Mod1 P2-20	IDE_RIRQ
22	GND	Mod0 P2-2	GND	Mod0 P2-1	IDE_RDAK#
23	FPGA3	Mod0 P2-4	D24	Mod0 P2-3	IDE_RRDY
24	GND	Mod0 P2-6	D25	Mod0 P2-5	IDE_RRD#
25	FPGA2	Mod0 P2-8	D26	Mod0 P2-7	IDE_RWR#
26	GND	Mod0 P2-10	D27	Mod0 P2-9	IDE_RDRQ
27	FPGA1	Mod0 P2-12	D28	Mod0 P2-11	IDE_RCS3#
28	GND	Mod0 P2-14	D29	Mod0 P2-13	IDE_RA[2]
29	Mod0 P2-23	Mod0 P2-16	D30	Mod0 P2-15	IDE_RRST#
30	GND	Mod0 P2-18	D31	Mod0 P2-17	+5V
31	Mod0 P2-24	Mod0 P2-20	GND	Mod0 P2-19	GND
32	GND	Mod0 P2-22	+5V	Mod0 P2-21	GND

Table 24. *Signal mnemonics of VMEbus rear I/O connector P2 – A15B – M-Modules*

	Signal	Direction	Function
Power	+5V	-	+5V power supply
	GND	-	Digital ground
VME64	A[31:24]	in	VME64 address lines
	D[31:16]	in/out	VME64 data lines
M-Module 2	MMod2 P2-*xx*	in/out	Signal *xx* from M-Module 2 rear I/O connector P2
M-Module 1	MMod1 P2-*xx*	in/out	Signal *xx* from M-Module 1 rear I/O connector P2
M-Module 0	MMod0 P2-*xx*	in/out	Signal *xx* from M-Module 0 rear I/O connector P2
IDE	+5V	-	+5 V power supply, current-limited to 1.5 A by a fuse
	GND	-	Digital ground
	IDE_RA[2:0]	out	IDE address [2:0]
	IDE_RACT#	in	IDE active
	IDE_RCS1#	out	IDE chip select 1
	IDE_RCS3#	out	IDE chip select 3
	IDE_RD[15:0]	in/out	IDE data [15:0]
	IDE_RDAK#	out	IDE DMA acknowledge
	IDE_RDRQ	in	IDE DMA request
	IDE_RIRQ	in	IDE interrupt request
	IDE_RRD#	out	IDE read strobe
	IDE_RRDY	in	IDE ready
	IDE_RRST#	out	IDE reset
	IDE_RWR#	out	IDE write strobe
FPGA	FPGA[8:1]	in/out	General-purpose I/O lines

Table 25. *Pin assignment of VMEbus rear I/O connector P2 – A15C – PMC*

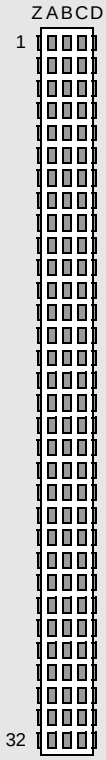
		Z	A	B	C	D
	1	-	PMC0 J14-2	+5V	PMC0 J14-1	-
	2	GND	PMC0 J14-4	GND	PMC0 J14-3	-
	3	-	PMC0 J14-6	-	PMC0 J14-5	-
	4	GND	PMC0 J14-8	A24	PMC0 J14-7	-
	5	-	PMC0 J14-10	A25	PMC0 J14-9	-
	6	GND	PMC0 J14-12	A26	PMC0 J14-11	-
	7	-	PMC0 J14-14	A27	PMC0 J14-13	-
	8	GND	PMC0 J14-16	A28	PMC0 J14-15	-
	9	-	PMC0 J14-18	A29	PMC0 J14-17	-
	10	GND	PMC0 J14-20	A30	PMC0 J14-17	-
	11	-	PMC0 J14-22	A31	PMC0 J14-21	-
	12	GND	PMC0 J14-24	GND	PMC0 J14-23	-
	13	-	PMC0 J14-26	+5V	PMC0 J14-25	-
	14	GND	PMC0 J14-28	D16	PMC0 J14-27	-
	15	-	PMC0 J14-30	D17	PMC0 J14-29	-
	16	GND	PMC0 J14-32	D18	PMC0 J14-31	-
	17	-	PMC0 J14-34	D19	PMC0 J14-33	-
	18	GND	PMC0 J14-36	D20	PMC0 J14-35	-
	19	-	PMC0 J14-38	D21	PMC0 J14-37	-
	20	GND	PMC0 J14-40	D22	PMC0 J14-39	-
	21	-	PMC0 J14-42	D23	PMC0 J14-41	-
	22	GND	PMC0 J14-44	GND	PMC0 J14-43	-
	23	-	PMC0 J14-46	D24	PMC0 J14-45	-
	24	GND	PMC0 J14-48	D25	PMC0 J14-47	-
	25	-	PMC0 J14-50	D26	PMC0 J14-49	-
	26	GND	PMC0 J14-52	D27	PMC0 J14-51	-
	27	-	PMC0 J14-54	D28	PMC0 J14-53	-
	28	GND	PMC0 J14-56	D29	PMC0 J14-55	-
	29	-	PMC0 J14-58	D30	PMC0 J14-57	-
	30	GND	PMC0 J14-60	D31	PMC0 J14-59	-
	31	-	PMC0 J14-62	GND	PMC0 J14-61	GND
	32	GND	PMC0 J14-64	+5V	PMC0 J14-63	-

Table 26. *Signal mnemonics of VMEbus rear I/O connector P2 – A15C – PMC*

	Signal	Direction	Function
Power	+5V	-	+5 V power supply
	GND	-	Digital ground
VME64	A[31:24]	in	VME64 address lines
	D[31:16]	in/out	VME64 data lines
PMC 0	PMC0 J14-*xx*	in/out	Signal *xx* from PMC 0 rear I/O connector J14

3 MENMON

3.1 General

MENMON is the CPU board firmware that is invoked when the system is powered on.

The basic tasks of MENMON are:

- Initialize the CPU and its peripherals.
- Load the FPGA code (if applicable).
- PCI auto configuration.
- Perform self-test.
- Provide debug/diagnostic features on MENMON command line.
- Boot operating system.
- Update firmware or operating system.

The following description only includes board-specific features. For a general description and in-depth details on MENMON 2nd Edition, please refer to the MENMON 2nd Edition User Manual.

3.1.1 State Diagram

Figure 11. *MENMON – State diagram, Degraded Mode/Full Mode*

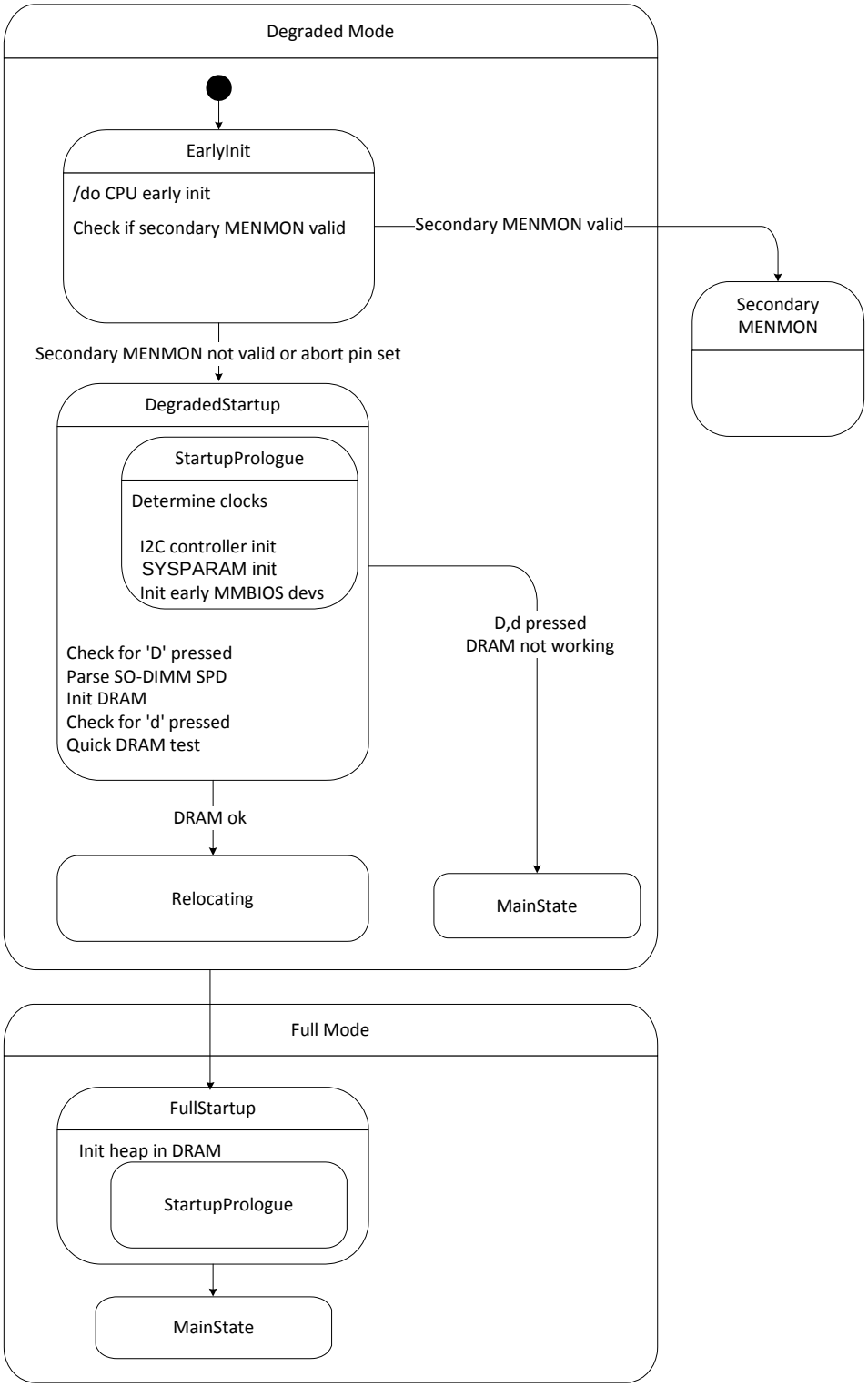
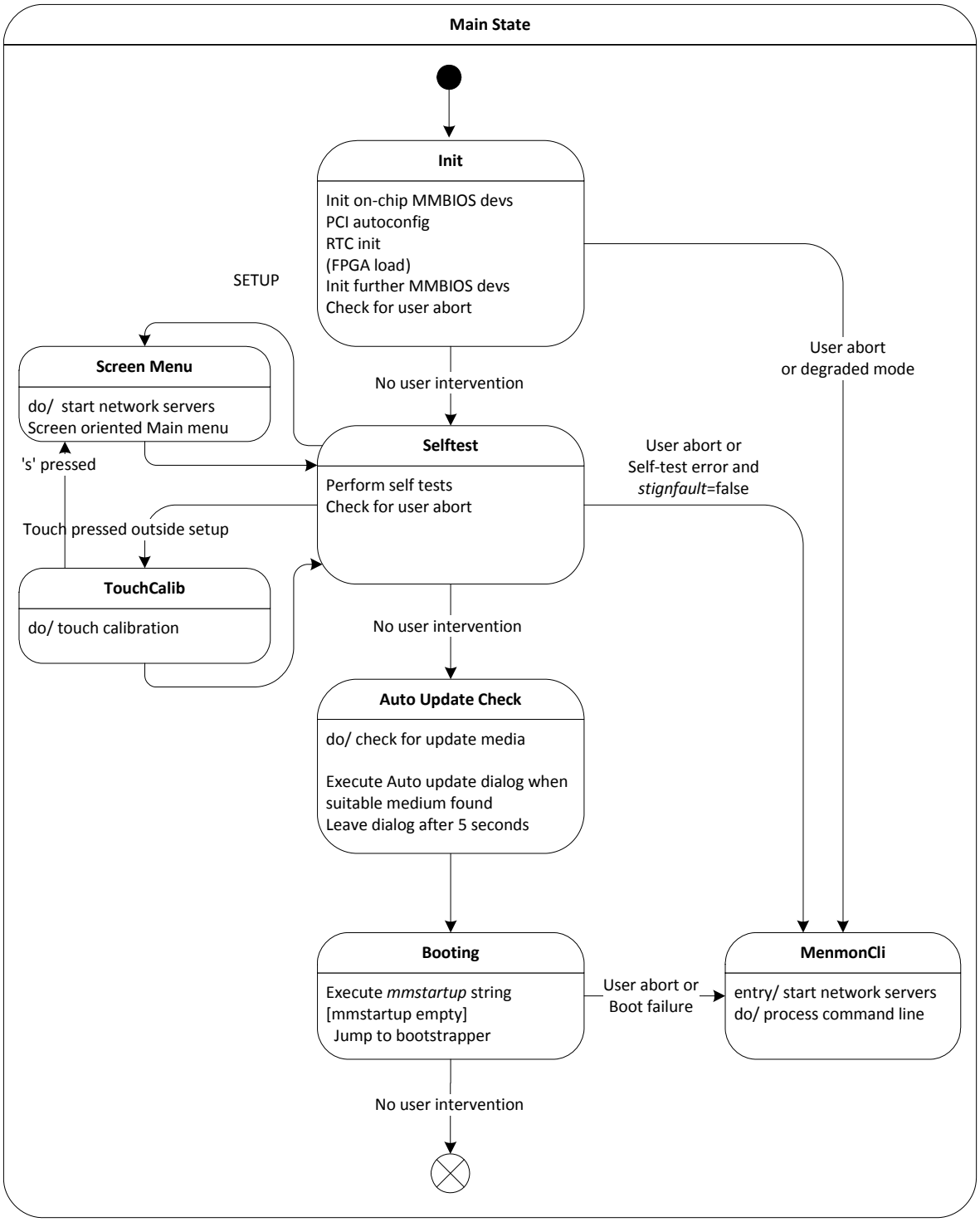


Figure 12. *MENMON – State diagram, main state*



3.2 Interacting with MENMON

To interact with MENMON, you can use the following consoles:

- UART COM1/2
- Telnet via network connection
- HTTP */monpage* via network connection

The default setting of the COM ports is 9600 baud, 8 data bits, no parity, and one stop bit.

3.2.1 Entering the Setup Menu/Command Line

During normal boot, you can abort the booting process in different ways during the self-test, depending on your console:

- With a text console press the "s" key to enter the Setup Menu.
- With a text console press "ESC" to enter the command line.

By default, the self-test is not left until 3 seconds have elapsed (measured from the beginning of the self-test), even if the actual test has finished earlier, to give the user a chance to abort booting and enter the Setup Menu.

You can modify the self-test wait time through MENMON system parameter *stwait* (see page 97).

3.3 Configuring MENMON for Automatic Boot

You can configure how MENMON boots the operating system either through the Setup Menu or through the command line.

In the Basic Setup Menu you can select the boot sequence for the bootable devices on the A15. The selected sequence is stored in system parameter *mmstartup* as a string of MENMON commands. For example, if the user selects: "Int. CF, Ether, (None)", the *mmstartup* string will be set to "DBOOT 0; NBOOT TFTP".

You can view and modify this string directly, using the Expert Setup Menu, option *Startup string*, or through the command-line command *EE-MMSTARTUP*.

(See also MENMON 2nd Edition User Manual for further details.)

3.4 Updating Boot Flash and CompactFlash

Please note that MENMON 2nd Edition as primary MENMON cannot start older versions as secondary (because older versions do not appear to have a valid header).

3.4.1 Update via the Serial Console using *SERDL*

You can use command *SERDL* to update program data using the serial console.

The following table shows the A15 locations:

Table 27. *MENMON – Program update files and locations*

File Name Extension	Typical File Name	Password for *SERDL*	Location
.PMM	*14A015-00_01_02.PMM*	MENMON	Primary MENMON
.SMM	*14A015-00_01_02.SMM*	MENMON	Secondary MENMON
.Axx	*MYFILE.A00*	-	Starting at byte *xx* in application Flash
.Fxxx	*MYFILE.F000*	-	Starting at sector *xxx* in boot Flash
.F10	*A015-IC56_R26.f10*	VME	VME FPGA
.Exx	*MYFILE.E00*	-	Starting at byte *xx* in EEPROM
.Dxx	*MYFILE.D00*	-	Starting at sector *xx* in SDRAM
.Cxx	*DSKIMG.C00*	DISK	Starting at sector *xx* in internal CompactFlash
.Sxx	*DSKIMG.B00*	DISK	Starting at sector *xx* in SCSI ID0

Table 28. *MENMON – Flash sectors for 32 MB application Flash*

Flash Sector	Address
0	0x0000000
1	0x0080000
2	0x0100000
3	0x0180000
.. (Sector offset 0x80000)	
62	0x1E80000
63	0x1F00000
64	0x1F80000

Table 29. *MENMON – Flash sectors for 2 MB boot Flash*

Flash Sector	Address
0	0x000000
1	0x010000
2	0x020000
3	0x030000
.. (Sector offset 0x10000)	
31	0x1F0000
32	0x1F8000
33	0x1FA000
34	0x1FC000

Table 30. *MENMON – Flash sectors for 4 MB boot Flash*

Flash Sector	Address
0	0x000000
1	0x010000
2	0x020000
3	0x030000
.. (Sector offset 0x10000)	
63	0x3F0000
64	0x3F2000
65	0x3F4000
66	0x3F6000
67	0x3F8000
68	0x3A0000
69	0x3C0000
70	0x3E0000

3.4.2 Update from Network using *NDL*

You can use the network download command *NDL* to download the update files from a TFTP server in network. The file name extensions, locations and passwords are the same as for the *SERDL* command.

3.4.3 Updating MENMON Code

Updates of MENMON are available for download from MEN's website. MENMON's integrated Flash update functions allow you to do updates yourself. However, you need to take care and follow the instructions given here. Otherwise, you may make your board inoperable!

In any case, read the following instructions carefully!

Please be aware that you do MENMON updates at your own risk. After an incorrect update your CPU board may not be able to boot.

WARNING: After a MENMON update, the hardware revision displayed by MENMON will most probably be different from the actual hardware revision of your CPU board, because MENMON follows MEN's hardware revision updates.

Do the following to update MENMON:

- ☑ Unzip the downloaded file, e.g. *14A015-00_01_02.zip*, into a temporary directory.
- ☑ Connect a terminal emulation program with the COM 1 port of your A15 and set the terminal emulation program to 9600 baud, 8 data bits, 1 stop bit, no parity, no handshaking (if you haven't changed the target baud rate on your own).
- ☑ Power on your A15, and press "ESC" immediately.
- ☑ In your terminal emulation program, you should see the "MenMon>" prompt.

If you are updating from MENMON version 1.xx to 2.xx, you need to update primary MENMON first:

- ☑ Enter "SERDL PMENMON" to update the primary MENMON. You should now see a "C" character appear every 3 seconds.
- ☑ In your terminal emulation program, start a "YModem" download of file *14A015-00_01_02.pmm* (for example, with Windows Hyperterm, select *Transfer > Send File* with protocol "YModem").
- ☑ When the download is completed, reset the A15.

In any case, continue as follows now to update the secondary MENMON:

- ☑ Enter "SERDL MENMON" to update the secondary MENMON. You should now see a "C" character appear every 3 seconds.
- ☑ In your terminal emulation program, start a "YModem" download of file *14A015-00_01_02.smm* (for example, with Windows Hyperterm, select *Transfer > Send File* with protocol "YModem").
- ☑ When the download is completed, reset the A15.

3.5 Diagnostic Tests

3.5.1 Ethernet

Table 31. *MENMON – Diagnostic tests: Ethernet*

Test Name	Description	Availability
ETHER0	Ethernet 0 internal loopback test Groups: POST AUTO	Always
ETHER1	Ethernet 1 internal loopback test Groups: POST AUTO	MENMON BIOS device "ETHER1" present
ETHER0_X	Ethernet 0 external loopback test Groups: NONAUTO ENDLESS	Always
ETHER1_X	Ethernet 1 external loopback test Groups: NONAUTO ENDLESS	MENMON BIOS device "ETHER1" present

3.5.1.1 Ethernet Internal Loopback Test

The test

- configures the network interface for loopback mode (on PHY)
- verifies that the interface's ROM has a good checksum
- verifies that the MAC address is valid (not `0xFFFFFF`...)
- sends 10 frames with `0x400` bytes payload each
- verifies that frames are correctly received on the same interface.

If the network interface to test is the currently activated interface for the MENMON network stack, the interface is detached from the network stack during test and reactivated after test.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY

Does not check:

- Connection between PHY and physical connector
- Interrupt line
- All LAN speeds

3.5.1.2 Ethernet External Loopback Test

This test is the same as the Ethernet Internal Loopback Test, but requires an external loopback connector. Before sending frames, the link state is monitored. If it is not ok within 2 seconds, the test fails.

Note: A loopback connector makes a connection between the following pins of the 8-pin Ethernet connector: 1-3, 2-6, 4-7, 5-8.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY
- Connection between PHY and physical connector

Does not check:

- Interrupt line
- All LAN speeds

3.5.2 SDRAM

Table 32. *MENMON – Diagnostic tests: SDRAM*

Test Name	Description	Availability
SDRAM	Quick SDRAM connection test Groups: POST AUTO	Always
SDRAM_X	Full SDRAM test Groups: NONAUTO ENDLESS	Always

3.5.2.1 Quick RAM Test

This quick test checks most of the connections to the RAM chips but does not test all RAM cells. It executes very quickly (within milliseconds).

This test is non-destructive (saves/restores original RAM content).

Checks:

- All address lines
- All data lines
- Byte enable signals
- Indirectly, checks clock and other control signals

Does not check:

- SDRAM cells
- SO-DIMM SPD EEPROM
- Burst mode

3.5.2.2 Extended RAM Test

This full-featured memory test allows to test all RAM cells. Depending on the size of the SO-DIMM, this test can take up to one minute.

It tests 8-, 16- or 32-bit access, each with random pattern, and single and burst access.

On each pass, this test first fills the entire memory (starting with the lowest address) with the selected pattern, using the selected access mode, and then verifies the entire block.

This test is destructive.

Checks:

- All address lines
- All data lines
- All control signals
- All SDRAM cells

Does not check:

- SO-DIMM SPD EEPROM

3.5.3 EEPROM

Table 33. *MENMON – Diagnostic tests: EEPROM*

Test Name	Description	Availability
EEPROM	I2C access/Magic nibble check Groups: POST AUTO	Always

This test reads the first EEPROM cell over SMB and checks if bits 3..0 of this cell contain the magic nibble `0xD`.

3.5.4 RTC

Table 34. *MENMON – Diagnostic tests: RTC*

Test Name	Description	Availability
RTC	Quick presence test of RTC Groups: POST AUTO	Always
RTC_X	Extended test of RTC Groups: NONAUTO ENDLESS	Always

3.5.4.1 RTC Test

This is a quick presence test of the real-time clock (RTC) and is executed on POST.

Checks:

- Presence of RTC (I²C access)

Does not check:

- If RTC is running
- RTC backup voltage

3.5.4.2 Extended RTC Test

Checks:

- Presence (e.g. I2C access)
- RTC is running

Does not check:

- RTC backup voltage

3.5.5 LM75

Table 35. *MENMON – Diagnostic tests: LM75*

Test Name	Description	Availability
LM75	Quick presence test of LM75 Groups: POST AUTO	Always

3.5.5.1 LM75 Test

This provides a quick presence test of the LM75 temperature sensor, which is executed during POST.

Checks:

- Presence of LM75 (I2C access)

Does not check:

- If temperature is correctly measured

3.6 MENMON Configuration and Organization

3.6.1 Consoles

You can select the active consoles by means of system parameters *con0..con3* and configure the console through parameters *ecl*, *gcon*, *hdp* and *tdp*. MENMON commands *CONS(-xxx)* also give access to the console settings (see Chapter 3.7 MENMON Commands (page 99)).

Table 36. *MENMON – System parameters for console selection and configuration*

Parameter (alias)	Description	Default	User Access
cbr (baud)	Baud rate of all UART consoles (decimal) (default: 9600 baud, 8n1)	9600	Read/write
con0..con3	CLUN of console 0..3 CLUN=0x00: disable CLUN=0xFF: Autoselect next available console *con0* is implicitly the debug console	*con0*: 04 (COM1) *con1*: 20 (VGA if card present)[1] *con2*: 00 (none) *con3*: 00 (none)	Read/write
ecl	CLUN of attached network interface (hex) CLUN=0x00: none CLUN=0xFF: first available Ethernet	0xFF	Read/write
gcon	CLUN of graphics device to display boot logo CLUN=0x00: disable CLUN=0xFF: Autoselect first available graphics console	0xFF (AUTO)	Read/write
hdp	HTTP server TCP port (decimal) 0: don't start telnet server -1: use default port 23 else: TCP port for telnet server	-1	Read/write
tdp	Telnet server TCP port (decimal) 0: don't start HTTP server -1: use default port 80 else: TCP port for HTTP server	-1	Read/write

[1] Legacy support for PC-MIP mezzanine modules.

3.6.2 Video Modes

None of the included drivers allows to change the video mode.

3.6.3 Abort Button

The abort button is available on the 40-pin I/O connector of the A15 (see Chapter 2.10 I/O Expansion Connector on page 42).

If the abort button is detected asserted, the secondary MENMON is not invoked. If you press the abort button for more than five seconds, the MENMON settings in the EEPROM are restored with default values. This is useful if a secondary MENMON has been programmed that does not work or if you have misconfigured a system parameter.

3.6.4 MENMON Memory Map

3.6.4.1 MENMON Memory Address Mapping

Figure 13. *MENMON Address Mapping*

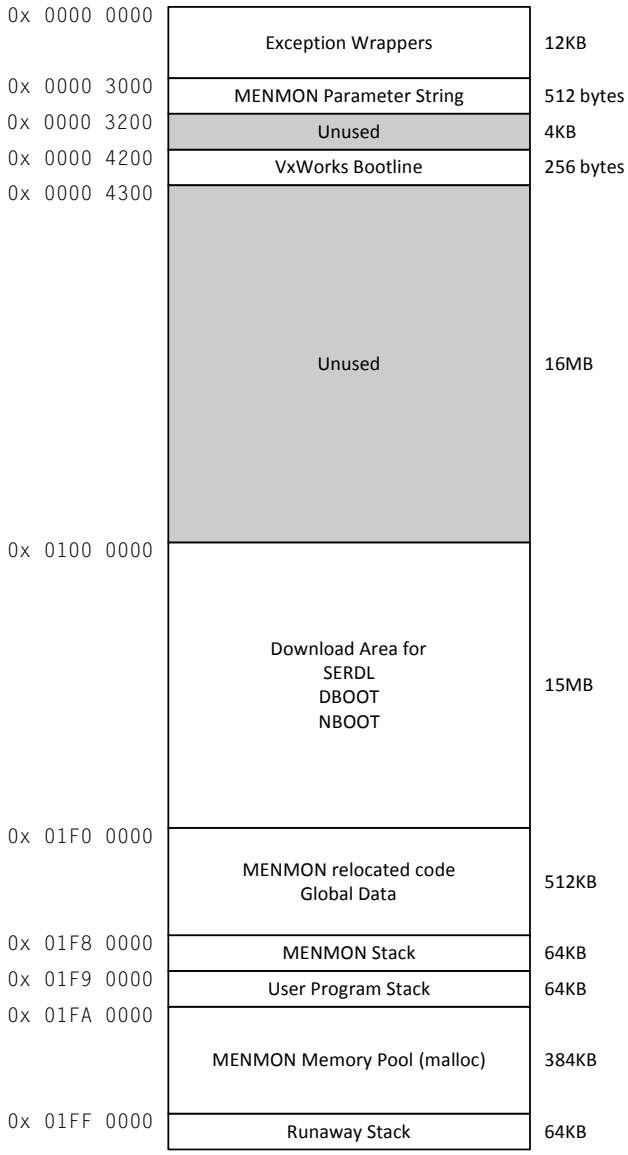


Table 37. MENMON – Address map (full-featured mode)

Address Space	Size	Description
0x 01F0 0000 .. 01F7 FFFF	512 KB	Text + Reloc
0x 01F8 0000 .. 01F8 FFFF	64 KB	Stack
0x 01F9 0000 .. 01F9 FFFF	64 KB	Stack for user programs
0x 01FA 0000 .. 01FF FFFF	384 KB	Heap1
0x 0190 0000 .. 01EF FFFF	6 MB	Heap2

3.6.4.2 Boot Flash Memory Map

The following shows the memory map for the 2-MB boot Flash:

Table 38. MENMON – Boot Flash memory map (2 MB)

Address Space	Description
0x FFE0 0000 .. FFEF FFFF	Available for OS
0x FFF0 0000 .. FFF7 FFFF	Primary MENMON
0x FFF8 0000 .. FFFF FFFF	Secondary MENMON

3.6.5 MENMON BIOS Logical Units

The following table shows fixed assigned CLUNs. All other CLUNs are used dynamically.

Table 39. MENMON – Controller Logical Units (CLUNs)

CLUN	MENMON BIOS Name	Description
0x00	IDE0	Primary IDE controller in ALI
0x01	IDE1	Secondary IDE controller in ALI
0x02	ETHER0	Onboard Ethernet #0 (LAN1)
0x03	ETHER1	Onboard Ethernet #1 (LAN2)
0x04	COM1	DUART8245 channel #0
0x05	COM2	DUART8245 channel #1
0x06	COM3	DUART8245 channel #2
0x07	COM4	DUART8245 channel #3
0x10	CONSOLE4	PS2 keyboard
0x20		All other devices dynamically detected
0x40		Telnet console
0x41		HTTP monitor console

Table 40. MENMON – Device Logical Units (DLUNs)

CLUN/DLUN	Description
0x00/0x00	Internal CompactFlash
0x01/0x00	External IDE Interface

3.6.6 System Parameters

System parameters are parameters stored in EEPROM. Some parameters are automatically detected by MENMON (such as CPU type and frequency). The parameters can be modified through the *EE-xxx* command via the command line.

3.6.6.1 Backward Compatibility of Parameters

MENMON 2nd Edition for the A15 is backward-compatible to older MENMON versions:

- Existing EEPROM sections are kept unchanged.
- A new EEPROM section (*menmx_parms*) has been added at offset `0x310`.. `0x34F`.

3.6.6.2 Physical Storage of Parameters in Ethernet SROMs

On the A15, LAN1 and 2 provide their own SROM, the parameters *nspeedX* and *nmacX* appear as system parameters.

3.6.6.3 A15 System Parameters

Note: Parameters marked by "Yes" in section "Parameter String" are part of the MENMON parameter string.

A blue background marks parameters different/new to older MENMON versions.

Table 41. *MENMON – A15 system parameters – Autodetected parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
clun	MENMON controller unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
cons	Selected console. Board specific, for backward compatibility. Setup according to device name that is used for *con0*		Yes	Read-only
cpu	CPU type as ASCII string (e.g. "MPC8245")		Yes	Read-only
cpuclkhz	CPU core clock frequency (decimal, Hz)		Yes	Read-only
dlun	MENMON device unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
flash[0..n]	Boot Flash size (decimal, kilobytes)		Yes	Read-only
mem0	RAM size (decimal, kilobytes)		Yes	Read-only
mem1..n	Board-specific size of additional memory (carrier board SRAM)		Yes	Read-only
memclkhz	Memory clock frequency (decimal, Hz)		Yes	Read-only
mm	Info whether primary or secondary MENMON has been used for booting, either "smm" or "pmm"		Yes	Read-only

Parameter (alias)	Description	Standard Default	Parameter String	User Access
mmst	Status of diagnostic tests, as a string		Yes	Read-only
pciclkhz	PCI bus clock frequency (decimal, Hz)		Yes	Read-only
rststat	Reset status code as a string		Yes	Read-only

Table 42. *MENMON – A15 system parameters – Production data*

Parameter (alias)[1]	Description	Standard Default	Parameter String	User Access
brd	Board name	-	Yes	Read-only
brdmod	Board model "mm"	-	Yes	Read-only
brdrev	Board revision "xx.yy.zz"	-	Yes	Read-only
sernbr	Board serial number	-	Yes	Read-only

[1] Parameters for production data of carrier boards will use prefixed parameter names, e.g. *c-brd*.

Table 43. *MENMON – A15 system parameters – Persistent parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
bsadr (bs)	Bootstrapper address. Used when *BO* command was called without arguments. (hexadecimal, 32 bits)	0	No	Read/write
cbr (baud)	Baudrate of all UART consoles (dec)	9600	Yes	Read/write
con0..conN	CLUN of console 0..n. (hex)	See Chapter 3.6.1 Consoles on page 91	No	Read/write
ecl	CLUN of attached network interface (hex)	0xFF	No	Read/write
gcon	CLUN of graphics screen (hex) (see Chapter 3.6.1 Consoles on page 91)	0xFF = auto	No	Read/write
hdp	HTTP server TCP port (decimal)	-1	No	Read/write
kerpar	Linux Kernel Parameters (399 chars max)	Empty string	No	Read/write
ldlogodis	Disable load of boot logo (bool)	0	No	Read/write
mmstartup (startup)	Start-up string (511 chars max)	Empty string	No	Read/write
nmacX	MAC address of Ethernet interface x (0..n). Format e.g. "00112233445566". Stored in dedicated ROM of Ethernet device.	0xFFFFFFFFFFFF	Yes	Read/write
nobanner	Disable ASCII banner on start-up	0	No	Read/write
nspeedX	Speed setting for Ethernet interface x (0..n). Stored in dedicated ROM of Ethernet device. Possible values: *AUTO*, *10HD*, *10FD*, *100HD*, *100FD*	AUTO	Yes	Read/write

Parameter (alias)	Description	Standard Default	Parameter String	User Access
selftest	For backward compatibility. All self-test flags (hex)	0		Read/write
stdis	Disable POST (bool)	0	No	Read/write
stignfault	Ignore POST failure, continue boot (bool)	0	No	Read/write
stwait	Time in 1/10 seconds to stay at least in SELFTEST state (decimal) 0 = Continue as soon as POST has finished	30	No	Read/write
tdp	Telnet server TCP port (decimal)	-1	No	Read/write
tries	Number of network tries	20	No	Read/write
tto	Minimum timeout between network retries (decimal, in seconds)	0	No	Read/write
u00..u15	User parameters (hex, 16 bits)	0x0000	No	Read/write
updcdis	Disable auto update check (bool)	0	No	Read/write
useflpar	Store *kerpar* and *mmstartup* parameters in boot Flash rather than in EEPROM (bool)	0	No	Read/write

Table 44. *MENMON – A15 system parameters – VxWorks bootline parameters*

Parameter (alias)	Description	Standard Default	Parameter String	User Access
bf (bootfile)	Boot file name (127 chars max)	Empty string	No	Read/write
bootdev	VxWorks boot device name	Empty string	No	Read/write
e (netip)	IP address, subnet mask, e.g. 192.1.1.28:ffffff00	Empty string	No	Read/write
g (netgw)	IP address of default gateway	Empty string	No	Read/write
h (nethost)	Host IP address (used when booting over *NBOOT TFTP*)	Empty string	No	Read/write
hostname	VxWorks name of boot host	Empty string	No	Read/write
netaddr	Access the IP address part of *netip* parameter		No	Read/write
netsm	Access the subnet mask part of *netip* parameter		No	Read/write
procnum	VxWorks processor number (decimal)	0	No	Read/write
s	VxWorks start-up script	Empty string	No	Read/write
tn (netname)	Host name of this machine	Empty string	No	Read/write
unitnum	VxWorks boot device unit number (decimal)	0	No	Read/write

3.6.6.4 VMEbus Configuration

There are some configuration commands available for the VME interface. Please note that the CPU address mapping to access the VMEbus from the board does not need to be configured (see Chapter 4 Organization of the Board on page 102).

EE-VME-IRQ <mask> – Configuring the interrupt handler

This command controls which of the seven VME interrupt levels should be enabled and should be handled by the board. Each bit in <mask> corresponds to one interrupt level (bit7 = level 7, bit1 = level 1).

For example *EE-VME-IRQ 0x30* would enable levels 5 and 4.

Bit 0 in <mask> controls enabling of the special ACFAIL interrupt.

Note: MENMON will never enable any interrupt in the VME bridge. The *EE-VME-IRQ* command is only here to provide a common way to enable interrupt levels for all operating systems. The operating system is responsible for reading the setting made by *EE-VME-IRQ* and for enabling the corresponding interrupts. The operating system has to read either the MENMON parameter string (cf. Chapter 3.6.6 System Parameters on page 95) or the EEPROM.

EE-VME-A24SA <val> – Configuring the VME slave address

The VME address of the board's shared SRAM can be configured through the *EE-VME-A24SA* command. <val> configures A23..A20 of the compare address, in steps of 1MB. For example *EE-VME-A24SA 8* configures a compare address of 0x800000.

Specifying *EE-VME-A24SA FF* disables access to the SRAM from VMEbus.

By default, the slave interface is disabled.

EE-VME-REQ <val> – Configuring the VMEbus requester method

The VME bus requester can be configured to ROR (release on request) or RWD (release when done):

- *EE-VME-REQ 0* Requester configured for ROR (default)
- *EE-VME-REQ 1* Requester configured for RWD

EE-VME-A32MA <val> – Configuring the VMEbus master prefix

<val> configures the upper three bits of the address on the VMEbus of the A32 CPU to VME window, e.g. 0x2000 0000.

3.7 MENMON Commands

The following table gives all MENMON commands that can be entered on the A15 MENMON prompt. You can call this list also using the *H* command.

Table 45. *MENMON – Command reference*

Command	Description
.[<reg>] [<val>]	Display/modify registers in debugger model
ARP	Dump network stack ARP table
AS <addr> [<cnt>]	Assemble memory
B[DC<no>] [<addr>]	Set/display/clear breakpoints
BIOS_DBG <mask> [net] | cons <clun>	Set MENMON BIOS or network debug level, set debug console
BO [<addr>] [<opts>]	Call OS bootstrapper
BOOTP [<opts>]	Obtain IP config via BOOTP
C[BWLLNAX#] <addr> [<val> ...]	Change memory
CHAM [<clun>]	Dump FPGA Chameleon table
CHAM-LOAD [<addr>]	Load FPGA
CONS	Show active consoles
CONS-ACT <clun1> [<clun2>] ...	Test console configuration
CONS-BAUD <baud>	Change baud rate instantly without storing
CONS-GX <clun>	Test graphics console
D [<addr>] [<cnt>]	Dump memory
DBOOT [<clun>] [<dlun>] [<opts>]	Boot from disk
DCACHE OFF | ON	Enable/disable data cache
DI [<addr>] [<cnt>]	Disassemble memory
DIAG [<which>] [VTF]	Run diagnostic tests
DSKRD <args>	Read blocks from RAW disk
DSKWR <args>	Write blocks to RAW disk
EE[-xxx] [<arg>]	Persistent system parameter commands
EER[-xxx] [<arg>]	Raw serial EEPROM commands
ERASE <D> [<O>] [<S>]	Erase Flash sectors
ESMCB-xxx	ESM carrier commands
FI <from> <to> <val>	Fill memory (byte)
GO [<addr>]	Jump to user program
H HELP	Print help
I [<D>]	List board information
ICACHE OFF | ON	Enable/disable instruction cache
IOI	Scan for BIOS devices

Command	Description
LOGO	Display MENMON start-up text screen
LS <clun> <dlun> [<opts>]	List files/partitions on device
MC <addr1> <addr2> <cnt>	Compare memory
MII <clun> [<reg>] [<val>]	Ethernet MII register command
MO <from> <to> <cnt>	Move (copy) memory
MS <from> <to> <val>	Search pattern in memory
MT [<opts>] <start> <end> [<runs>]	Memory test
NBOOT [<opts>]	Boot from Network
NDL [<opts>]	Update Flash from network
NETSTAT	Show current state of networking parameters
PCI	PCI probe
PCIC <dev> <addr> [<bus>] [<func>]	PCI config register change
PCID[+] <dev> [<bus>] [<func>]	PCI config register dump
PCIR	List PCI resources
PCI-VPD[-] <devNo> [<busNo>] [<capId>]	PCI Vital Product Data dump
PFLASH <D> <O> <S> [<A>]	Program Flash
PGM-XXX <args>	Media copy tool
PING <host> [<opts>]	Network connectivity test
RBOOT	Boot from shared RAM
RST	Cause an instant system reset
RTC[-xxx] [<arg>]	Real time clock commands
S [<addr>]	Single step user program
SERDL [<passwd>]	Update Flash using YModem protocol
SETUP	Open interactive Setup menu
WDOG-TOUT <value>	Set watchdog timeout in ms

3.7.1 User LEDs

There are two LEDs available on the I/O connector (see Chapter 2.10 I/O Expansion Connector on page 42). The LEDs display the state of the boot like a counter.

The exact sequence of the LEDs, i. e. when each LED will light, depends on the MENMON version. If you have any problems during start-up, please turn to MEN's support and give your MENMON version.

3.7.2 Watchdog Configuration

By default, the board watchdog is disabled.

The watchdog can be enabled through *WDOG-TOUT <ms>* where <ms> specifies the watchdog timeout in milliseconds. Possible values are 0 (disable watchdog), 800, 1600, 3200, and 6400.

Once the watchdog is enabled, it must be served by toggling the ALI GPO22 pin. If the software fails to toggle this pin in time, the CPU is reset.

MENMON automatically and continuously serves the watchdog until the operating system is started.

3.7.3 Hex Switch

The hex switch is completely user-configurable. With MENMON it has only one function: at hex position "0" or "8" there will be a delay after each initialization step, so that the boot procedure is slowed down. This function is provided for diagnostic purposes. For normal operation of the board, you should set the hex switch to a position between "1" and "F".

Table 46. *Hex-switch settings*

Setting	Description
0	User-defined, but delay after each initialization step
1..F	User-defined, no additional delay during boot

4 Organization of the Board

To install software on the board or to develop low-level software it is essential to be familiar with the board's address and interrupt organization.

4.1 Memory Mappings

The memory mapping of the board complies with the PowerPC CHRP (Common Hardware Reference Platform) Specification. The integrated host-to-PCI bridge is set to map B to support this mapping.

4.1.1 Processor View of the Memory Map

Table 47: *Memory Map - Processor View*

CPU Address Range	Size	Description
0x 0000 0000..0FFF FFFF	1 GB	DRAM
0x 7000 0000..7001 FFFF	128 KB	FPGA Load Latch
0x 7800 0000..7CFF FFFF	32 MB	Application Flash
0x 8000 0000..87FF FFFF	128 MB	M-Module Bridge, PCI Memory Space
0x 8800 0000..88FF FFFC	16 MB	VME A24 D16 (standard) space **swapped**
0x 8900 0000..8900 FFFC	64 KB	VME A16 D16 (short) space **swapped**
0x 8901 0000..8901 FFFC	64 KB	VME A16 D32 (short) space **swapped**
0x 8940 0000..894F FFFC	1 MB	Local SRAM
0x 8980 0000..8980 0044	72 bytes	VME Bridge Control Registers
0x 8980 0800..8980 0FFC	2 KB	VME Bridge Internal RAM
0x 89C0 0000	16 bytes	VME IACK space **swapped**
0x 8A00 0000..8A0F FFFF	1 MB	8245 EUMB, PCI Memory Space
0x 8C00 0000..8CFF FFFC	16 MB	VME A24 D32 (standard) space **swapped**
0x 8D00 0000..8DFF FFFC	16 MB	VME A24 D32 (standard) space
0x 8DFF FFFD..9FFF FFFF	288 MB	Auto mapping, PCI Memory Space
0x A000 0000..BFFF FFFF	512 MB	VME A32 D32 (long) space **swapped**, PCI Memory Space
0x C000 0000..DFFF FFFC	512 MB	VME A32 D32 (long) space
0x DFFF FFFD..FCFF FFFF	464 MB	No auto mapped PCI Memory Space
0x E000 0000..E0FF FFFC	16 MB	VME A24 D16 (standard) space

CPU Address Range	Size	Description
0x E100 0000..E100 FFFC	64 KB	VME A16 D16 (short) space
0x E101 0000..E101 FFFC	64 KB	VME A16 D32 (short) space
0x E140 0000..E14F FFFC	1 MB	Local SRAM
0x E180 0000..E180 0044	72 bytes	VME Bridge Control Registers
0x E180 0800..E180 0FFC	2 KB	VME Bridge Internal RAM
0x FD00 0000..FDFF FFFF	16 MB	PCI ISA Memory Space PCI/ISA Addr.: 0x 0000 0000..00FF FFFF
0x FE00 0000..FE00 FFFF	64 KB	PCI ISA I/O Space
0x FE80 0000..FEBF FFFF	4 MB	PCI I/O Space (not used)
0x FEC0 0000..FEDF FFFF	2 MB	PCI Config Addr. Reg.
0x FEE0 0000..FEEF FFFF	1 MB	PCI Config Data. Reg.
0x FEF0 0000..FEFF FFFF	1 MB	PCI IACK Space
0x FFE0 0000..FFFF FFFF	2 MB	Boot Flash (8 Bit)

Table 48. *Address Mapping for PCI*

Address Range	Size	Description
PCI Memory Space (addresses as seen on PCI bus)		
0x 8000 0000..87FF FFFF		M-Module bridge
0x 8800 0000..89FF FFFF		VMEbus bridge
0x 8A00 0000..8A0F FFFF		MPC8245 Embedded utility block
0x 8B00 0000..9FFF FFFF		Available for PCI auto-configuration
PCI I/O Space (addresses as seen on PCI bus)		
0x 0000..21FF		Fixed addresses of ISA devices (see Chapter 4.1.2 PCI/ISA I/O Space Memory Map on page 105)
0x 2200..EFFF		Available for PCI I/O space auto-configuration
0x F000..FFFF		ALI IDE bus mastering

Table 49. *BATS set up by MENMON*[1]

Addr	BAT	Description
0x F000 0000..FFFF FFFF	0	PCI ISA & I/O & IACK and boot Flash IBAT: Caching enabled
0x 0000 0000..*xx*00 0000 (depending on DRAM configuration)	1	DRAM IBAT: Caching enabled
0x 8000 0000..8FFF FFFF	2	PCI Memory Space
0x A000 0000..BFFF FFFF	3	PCI Memory Space / will be temporarily swapped to 0x7000 0000 for FPGA Load access or Application Flash Access or to 0xE000 0000 for swapped VME access

[1] Unless otherwise stated, all BATS are initialized with W I M !G.

4.1.2 PCI/ISA I/O Space Memory Map

This memory map complies to the ISA I/O address assignments. Refer to data sheet "ALADDIN M1543: Desktop South Bridge, version 1.25, Jan. 1998" for configuration registers.

Table 50. *PCI/ISA I/O Space Memory Map (addresses as seen from CPU)*

CPU Address Range	Device	Register
0x FE00 0000..FE00 000F	M1543	DMA1 (slave)
0x FE00 0020	M1543	INT_1 (master) Control Register
0x FE00 0021	M1543	INT_1 (master) Mask Register
0x FE00 0040	M1543	Timer Counter - Channel 0 Count
0x FE00 0041	M1543	Timer Counter - Channel 1 Count
0x FE00 0042	M1543	Timer Counter - Channel 2 Count
0x FE00 0043	M1543	Timer Counter Command Mode Register
0x FE00 0060	M1543	Read_access Clear IRQ[12] (for PS2), IRQ[1] Latched Status
0x FE00 0060	M1543	Keyboard Data Buffer
0x FE00 0061	M1543	NMI and Speaker Status and Control
0x FE00 0064	M1543	Keyboard Status(R)/Command(W)
0x FE00 0080..FE00 009F	M1543	DMA Channel x Page Register
0x FE00 00A0	M1543	INT_2 (slave) Control Register
0x FE00 00A1	M1543	INT_2 (slave) Mask Register
0x FE00 00C0..FE00 00DF	M1543	DMA2 (master)
0x FE00 00F0	M1543	Coprocessor Error Ignored Register
0x FE00 0170..FE00 0177	M1543	IDE Secondary registers part A
0x FE00 01F0..FE00 01F7	M1543	IDE Primary registers part A
0x FE00 02F8..FE00 02FF	M1543 Super I/O	UART2 controller
0x FE00 0378..FE00 037F	M1543 Super I/O	Parallel Port Controller
0x FE00 03F0	M1543 Super I/O	Config Port Index
0x FE00 03F1	M1543 Super I/O	Config Port Data
0x FE00 0376..FE00 0377	M1543	IDE Secondary registers part B
0x FE00 03F6..FE00 03F7	M1543	IDE Primary registers part B
0x FE00 03F8..FE00 03FF	M1543 Super I/O	UART1 controller
0x FE00 040B	M1543	DMA1 Extended Mode Register
0x FE00 0481..FE00 048B	M1543	DMA High Page Registers
0x FE00 04D0	M1543	INT_1 (master) Edge/Level Control
0x FE00 04D1	M1543	INT_2 (slave) Edge/Level Control
0x FE00 04D6	M1543	DMA2 Extended Mode Register
0x FE00 0CF8	MPC106	PCI Config Space Index
0x FE00 0CFC	MPC106	PCI Config Space Data
0x FE00 1800..FE00 181E	M1543	SMB Controller

4.2 Interrupt Handling

The board supports both maskable and nonmaskable interrupts. The interrupt controller is located inside the M1543 PCI-to-ISA bridge.

Table 51. *Interrupts on the CPU Board*

Interrupt	Active Polarity	Edge/Level	Source
0	High	Edge	Timer/Counter 0
1	High	Edge	Keyboard
3	High	Edge	COM2
4	High	Edge	COM1
7	Low	Level	PCI INTA
8	Low	Edge	ABORT OR CompactPCI ENUM
9	Low	Level	Reserved for FPGA user IRQ
10	Low	Level	PCI INTB (M-Modules + VME bridge)
11	Low	Level	PCI INTC, PCI INTD (Ethernet 1, Ethernet 2)
12	High	Edge	Mouse
13			Not usable (Coprocessor INT in PC environment)
14	High	Edge	Primary IDE (CompactFlash) SIRQ1
15	High	Edge	Secondary IDE (Std IDE) SIRQ2

4.2.1 Nonmaskable Interrupts

The M1543 can be programmed to assert an NMI when it detects a low level of the SERR# line on the PCI local bus. The integrated host-to-PCI bridge will assert MCP# to the processor upon detecting a high level on NMI from the M1543. The host-to-PCI bridge can also be programmed to assert MCP# under other conditions. Please refer to the respective user manual for details.

4.2.2 Maskable Interrupts

The M1543 supports 15 interrupt requests. These 15 interrupts are ISA-type interrupts that are functionally equivalent to two 82C59 interrupt controllers. The chip also provides two steerable IRQ lines which can be routed to any of the available ISA interrupts. The M1543 supports four PCI interrupts: INTA#, INTB#, INTC# and INTD#. The interrupt lines may to be routed to any of twelve ISA interrupt lines.

The entire interrupt routing is managed by the boot software and board support package of the operating system.

Note: The ALI1543C PIC handles all interrupts. The MPC8245's EPIC is not used!

4.3 Implementation of M1543 PCI-to-ISA Bridge

The GPO/GPI/GPIO pins of the M1543 are used for several functions on the board. The tables below show the port assignments of the board.

Table 52. *M1543 General Purpose Input (GPI) Pin Assignments*

GPI	Description
0	Abort button, ORed with ENUM signal
1	Reserved
2	LM75
3	PXI TRIG0

Table 53. *M1543 General Purpose Output (GPO) Pin Assignments*

GPO	Description
0	Reserved
1	PXI TRIG2
2	PXI TRIG3
3	Software reset
4..17	Reserved
18	PXI TRIG0
19	PXI TRIG1
20	SMB2 SCL
21	Reserved
22	Watchdog toggle (SMS24 WDI)

Table 54. *M1543 General Purpose Input/Output (GPIO) Pin Assignments*

GPIO	Direction	Description
0	in	Hex switch
1	in	Hex switch
2	out	Hex switch
3	in	Hex switch
4	in[1]/out	LED1 (front and I/O connector)
5	in[1]/out	LED2 (front and I/O connector)
6	out	Reserved
7	in/out	SMB2 SDA

[1] Optional if used via I/O connector. If you want to use the LEDs as inputs, please contact MEN's support.

4.4 SMB Devices

Two System Management Buses are used: SMB 1 is handled via the M1543 SMB controller, SMB 2 via the GPIOs of the M1543.

Table 55. *SMB 1 Devices*

Address	Function
0x A0	SPD of SO-DIMM
0x 9A	LM75
0x D0	RTC M41T56

Table 56. *SMB 2 Devices*

Address	Function
0x 9x	Config Regs of SMS24
0x Ax	Memory Array of SMS24

4.5 PCI Devices on Bus 0

Table 57. *PCI Devices on Bus 0*

Device Number	Vendor ID	Device ID	Function	Interrupt
0x 00	0x 1057	0x 0003	Integrated host-to-PCI bridge in MPC8245	-
0x 12	0x 10B9	0x 1533	M1543 PCI-to-ISA	-
0x 17	0x 8086	0x 1209	Ethernet 82559 I	PCI INTD
0x 18	0x 1172	0x 410C	MEN M-Module (optional)	PCI INTB
0x 19	0x 1172	0x 5056	MEN VME bridge	PCI INTB
0x 1B	0x 10B9	0x 5229	M1543 IDE	ISA 14, 15
0x 1C	0x 10B9	0x 7101	M1543 PMU	-
0x 1A	0x 8068	0x 1208	Ethernet 82559 II	PCI INTC
0x 1D	0x 0026	0x 3388	PCI-to-PMC bridge (optional)	-

4.6 PCI Devices on PMC Bus

Table 58. *PCI Devices on PMC Bus*

Device Number	Vendor ID	Device ID	Function	INTA led to
0x 03	Depends on mezzanine module		PMC 0	PCI INTA
0x 02			PMC 1	PCI INTD

4.7 M-Module Interface

The M-Module FPGA implements the access logic for three M-Modules. All devices are mapped via BAR0 (64MB).

Table 59. *M-Module Device Addresses*

Offset Address	Mapped by MENMON to	Function
0x 0000 0000	0x 8000 0000	M-Module 0
0x 0200 0000	0x 8200 0000	M-Module 1
0x 0400 0000	0x 8400 0000	M-Module 2
0x 0600 0000	0x 8600 0000	Reserved for FPGA user functions

For details on M-Module address spaces see Chapter 2.6.2 Addressing the M-Modules on page 32.

5 Appendix

5.1 Literature and Web Resources

- A15B data sheet with up-to-date information and documentation:
  www.men.de/products/01A015B.html
- A15C data sheet with up-to-date information and documentation:
  www.men.de/products/01A015C.html

5.1.1 PowerPC

- MPC8245:
  MPC8245 Integrated Processor User's Manual
  MPC8245UM; 2005; Freescale Semiconductor
  www.freescale.com

5.1.2 VMEbus

- VMEbus General:
  - The VMEbus Specification, 1989
  - The VMEbus Handbook, Wade D. Peterson, 1989

  VMEbus International Trade Association
  www.vita.com

5.1.3 PCI

- PCI Local Bus Specification Revision 2.2:
  1998; PCI Special Interest Group
  P.O. Box 14070
  Portland, OR 97214, USA
  www.pcisig.com

5.1.4 Bridges

- M1543 PCI-to-ISA bridge:
  M1543 Preliminary Data Sheet, Acer Laboratories Inc. Jan. 1998 / Version 1.25

5.1.5 M-Modules

- M-Module Standard:
  ANSI/VITA 12-1996, M-Module Specification;
  VMEbus International Trade Association
  www.vita.com

5.1.6 PMC

- PMC specification:
  Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, 1386.1; 1995; IEEE
  www.ieee.org

5.1.7 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE
  www.ieee.org
- Charles Spurgeon's Ethernet Web Site
  Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.
  www.ethermanage.com/ethernet/
- InterOperability Laboratory, University of New Hampshire
  This page covers general Ethernet technology.
  www.iol.unh.edu/services/testing/ethernet/training/

5.1.8 EIDE

- EIDE:
  Information Technology - AT Attachment-3 Interface (ATA-3), Revision 6, working draft; 1995; Accredited Standards Committee X3T10

5.1.9 USB

- USB Implementers Forum, Inc.
  www.usb.org

5.2 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the A15. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 14. *Labels giving the board's article number, revision and serial number*